NEHRU COLLEGE OF ENGINEERING AND RESEARCH CENTRE
(NAAC Accredited)
(Approved by AICTE, Affiliated to APJ Abdul Kalam Technological University, Kerala)

Moulding True Citizen
Since 1968

DEPARTMENT OF MECHATRONICS ENGINEERING

LAB MANUAL

MRL 203 ANALOG AND DIGITAL ELECTRONICS LAB

VISION OF THE INSTITUTION

To mould true citizens who are millennium leaders and catalysts of change through excellence in education.

MISSION OF THE INSTITUTION

NCERC is committed to transform itself into a center of excellence in Learning and Research in Engineering and Frontier Technology and to impart quality education to mould technically competent citizens with moral integrity, social commitment and ethical values.

We intend to facilitate our students to assimilate the latest technological know-how and to imbibe discipline, culture and spiritually, and to mould them in to technological giants, dedicated research scientists and intellectual leaders of the country who can spread the beams of light and happiness among the poor and the underprivileged.

ABOUT DEPARTMENT

- Established in: 2013
- Course offered: B.Tech Mechatronics Engineering
- Approved by AICTE New Delhi and Accredited by NAAC
- Affiliated to the University of A P J Abdul Kalam Technological University.

DEPARTMENT VISION

To develop professionally ethical and socially responsible Mechatronics engineers to serve the humanity through quality professional education.

DEPARTMENT MISSION

1) The department is committed to impart the right blend of knowledge and quality education to create professionally ethical and socially responsible graduates.

2) The department is committed to impart the awareness to meet the current challenges in technology.

3) Establish state-of-the-art laboratories to promote practical knowledge of mechatronics to meet the needs of the society

PROGRAMME EDUCATIONAL OBJECTIVES

I. Graduates shall have the ability to work in multidisciplinary environment with good professional and commitment.

II. Graduates shall have the ability to solve the complex engineering problems by applying electrical, mechanical, electronics and computer knowledge and engage in lifelong learning in their profession.

III. Graduates shall have the ability to lead and contribute in a team with entrepreneur skills, professional, social and ethical responsibilities.

IV. Graduates shall have ability to acquire scientific and engineering fundamentals necessary for higher studies and research.

PROGRAM OUTCOME (PO'S)

Engineering Graduates will be able to:

PO 1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO 2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO 3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO 4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO 5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO 6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO 7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO 8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO 9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO 10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO 11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO 12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOME(PSO'S)

PSO 1: Design and develop Mechatronics systems to solve the complex engineering problem by integrating electronics, mechanical and control systems.

PSO 2: Apply the engineering knowledge to conduct investigations of complex engineering problem related to instrumentation, control, automation, robotics and provide solutions.

MRL 203	ANALOG AND DIGITAL ELECTRONICS LAB	CATEGORY	L	T	P	CREDIT
		PCC	-	-	3	2

Preamble: This lab course is intended to impart working knowledge and design skills in analog and digital circuits. It also helps the students to demonstrate various applications in analog and digital circuits.

Prerequisite: ESL130 Electronics Workshop

Course Outcomes: After the completion of the course the student will be able to

CO 1	Set up an experiment to obtain the characteristics of BJT and FET.
CO 2	Acquire skills in designing and testing various applications of analog and digital integrated circuits
CO 3	Analyse and interpret the circuits using the softwares which are available for complex design methodologies.
CO 4	Design and implement analog and digital modules based on specifications.
CO 5	Enhance the ability to function effectively as an individual and in a team to accomplish the given task.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3	3	2	-	2	1	-	-	3	2	-	2
CO 2	3	3	3	3	2	1	1	1	3	2	2	3
CO 3	2	2	2	3	3	1	1	1	3	2	2	2
CO 4	3	3	2	2	2	1	1	1	3	2	2	2
CO 5	1	2	2	2	2	1	1	3	3	2	2	2

Assessment Pattern

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	75	75	2.5 hours

Continuous Internal Evaluation Pattern:

Attendance : 15 marks
Continuous Assessment : 30 marks
Internal Test (Immediately before the second series test) : 30 marks

End Semester Examination Pattern: The following guidelines should be followed regarding award of marks

(a) Preliminary work : 15 Marks
(b) Implementing the work/Conducting the experiment : 10 Marks
(c) Performance, result and inference (usage of equipments and trouble shooting) : 25 Marks
(d) Viva voce : 20 marks
(e) Record : 5 Marks

General instructions: Practical examination to be conducted immediately after the second series test covering entire syllabus given below. Evaluation is a serious process that is to be conducted under the equal responsibility of both the internal and external examiners. The number of candidates

evaluated per day should not exceed 20. Students shall be allowed for the University examination only on submitting the duly certified record. The external examiner shall endorse the record.

Course Assessment Questions

1. For the given JFET, find out the pinch off voltage.
2. Design an inverting amplifier of gain 10.
3. Design a circuit to obtain the following transfer characteristics.
4. Generate a waveform with 50% duty cycle using IC 555.
5. Determine the lock in range and capture range of IC 565.
6. Design a 3 bit synchronous counter.
7. Design a full adder and implement it with universal gates.
8. Design a 4 bitgray to binary code converter.
9. Implement an 8:1 multiplexer.
10. Set up an experiment to learn the working of shift registers.

LIST OF EXPERIMENTS (At least 14 of the following experiments)

Any 5 experiments can be simulated using SPICE, Proetus, Scilab, Verilog or Matlab; any relevant package may be used.

1. Characteristics of CE amplifier.
2. Characteristics of JFET/MOSFET.
3. Design of RC Phase shift oscillator using BJT.
4. Study the characteristics of operational amplifier IC 741.
5. Inverting, non inverting amplifier and voltage follower.
6. Design of Differentiator / Integrator and Schmitt Trigger.
7. Design of Astable/monostable using IC 555.

8. Study the response of active first order LPF and HPF filters.
9. Design of PLL.
10. Study and Verify the truth tables of logic gates and flip flops.
11. Design and implementation of 3 bit full adder and subtractor.
12. Design and implementation of code converters using logic gates
    i. Binary to gray and Gray to Binary Code converter.
    ii. BCD to Excess 3 code and Excess 3 to BCD converter.
13. Design and implement Multiplexer and De-multiplexer using logic gates.
14. Design and implement encoder and decoder using logic gates.
15. Implementation of SISO, SIPO, PISO and PIPO shift registers using Flip- flops.
16. Design and implementation of 3bit synchronous and asynchronous counters
17. Construction and verification of 4bit Mod-10/Mod-12 Ripple counters.

Text Books

1. K A Navas, "Electronics Lab Manual-volume 1",PHI Learning Private Limited,2015.

Reference Books

1. Franco S., "Design with Operational Amplifiers and Analog Integrated Circuits", 3/e, Tata McGraw Hill, 2008
2. David A. Bell, "Operational Amplifiers & Linear ICs", Oxford University Press, 2ndedition, 2010.
3. Donald DGivone, "Digital Principles and Design", Tata McGraw Hill, 2003.

PREPARATION FOR THE LABORATORY SESSION

GENERAL INSTRUCTIONS TO STUDENTS

1. Read carefully and understand the description of the experiment in the lab manual. You may go to the lab at an earlier date to look at the experimental facility and understand it better. Consult the appropriate references to be completely familiar with the concepts and hardware.

2. Make sure that your observation for previous week experiment is evaluated by the faculty member and your have transferred all the contents to your record before entering to the lab/workshop.

3. At the beginning of the class, if the faculty or the instructor finds that a student is not adequately prepared, they will be marked as absent and not be allowed to perform the experiment.

4. Bring necessary material needed (writing materials, graphs, calculators, etc.) to perform the required preliminary analysis. It is a good idea to do sample calculations and as much of the analysis as possible during the session. Faculty help will be available. Errors in the procedure may thus be easily detected and rectified.

5. Please actively participate in class and don't hesitate to ask questions. Please utilize the teaching assistants fully. To encourage you to be prepared and to read the lab manual before coming to the laboratory, unannounced questions may be asked at any time during the lab.

6. Carelessness in personal conduct or in handling equipment may result in serious injury to the individual or the equipment. Do not run near moving machinery/equipment. Always be on the alert for strange sounds. Guard against entangling clothes in moving parts of machinery.

7. Students must follow the proper dress code inside the laboratory. To protect clothing from dirt, wear a lab coat. Long hair should be tied back. Shoes covering the whole foot will have to be worn.

8. In performing the experiments, please proceed carefully to minimize any water spills, especially on the electric circuits and wire.

9. Maintain silence, order and discipline inside the lab. Don't use cell phones inside the laboratory.

10. Any injury no matter how small must be reported to the instructor immediately.

11. Check with faculty members one week before the experiment to make sure that you have the handout for that experiment and all the apparatus.

AFTER THE LABORATORY SESSION

1. Clean up your work area.

2. Check with the technician before you leave.

3. Make sure you understand what kind of report is to be prepared and due submission of record is next lab class.

4. Do sample calculations and some preliminary work to verify that the experiment was successful

MAKE-UPS AND LATE WORK

Students must participate in all laboratory exercises as scheduled. They must obtain permissionfrom the faculty member for absence, which would be granted only under justifiablecircumstances. In such an event, a student must make arrangements for a make-up laboratory, which will be scheduled when the time is available after completing one cycle. Late submission will be awarded less mark for record and internals and zero in worst cases.

LABORATORY POLICIES

1. Food, beverages & mobile phones are not allowed in the laboratory at any time.

2. Do not sit or place anything on instrument benches.

3. Organizing laboratory experiments requires the help of laboratory technicians and staff. Be punctual.

INDEX

ADDITIONAL/ADVANCED EXPERIMENTS		
1	HALF ADDER	81
2	HALF SUBTRACTOR	84

VERIFICATION BY HOD

INTERNAL EXAMINER

EXTERNAL EXAMINER

EXPERIMENT NO : 1

CHARACTERISTICS OF CE AMPLIFIER

Aim: To design and setup an RC Coupled amplifier using BJT & to find the input and output impedance of the RC-Coupled amplifier.

Components Required:

- Transistor
- Capacitor
- Resistors
- Signal Generator
- CRO

Design:

Let Vcc = 10V

Ic = 5mA

β = 100

To find RE:

$$V_{RE} = \frac{Vcc}{10} = \frac{10}{10} = 1V$$

i.e. $I_E R_E = 1V$

$$R_E = \frac{1V}{I_E} = \frac{1V}{I_C} = \frac{1V}{5mA} = 200\Omega$$

Select $R_E = 220\Omega$

To find R_C:

$$V_{CE} = \frac{Vcc}{2} = \frac{10}{2} = 5V$$

Apply KVL to CE loop,

$$V_{CC} - I_C R_C - V_{CE} - V_{BE} = 0$$

$$10 - 5mR_C - 5 - 1 = 0$$

$$R_C = 800\Omega$$

Select R_C as 820 Ω

To find R_1:

From the above biasing circuit,

$$V_B = V_{BE} + V_{RE} = 0.7 + 1 = 1.7V$$

$$I_C = \beta I_B \text{ or } I_B = \frac{I_C}{\beta} = \frac{5m}{100} = 0.05mA$$

Assume 10 I_B flows through R_1

$$\therefore R_1 = \frac{Vcc - V_B}{10\ I_B} = \frac{10 - 1.7}{10 \times 0.050}$$

$$R_1 = 16.6K\Omega$$

Select R_1 as $18K\Omega$

Assume 9 I_B flows through R2

$$\therefore R_2 = \frac{V_B}{9\ I_B} = \frac{1.7}{9 \times 0.050m} = 3.7K\Omega$$

Select R_2 as $3.9K\Omega$

Bypass capacitor C_E and coupling Capacitor C_{C1} and C_{C2}

Let $X_{CE} = \frac{1}{10} R_E$ at f = 100Hz

i.e. $\frac{1}{2\pi f C_E} = \frac{R_E}{10}$

$$\therefore C_E = \frac{10}{2\pi \times 100 \times 220} = 72.3\mu F$$

Select C_E as $100\mu F$

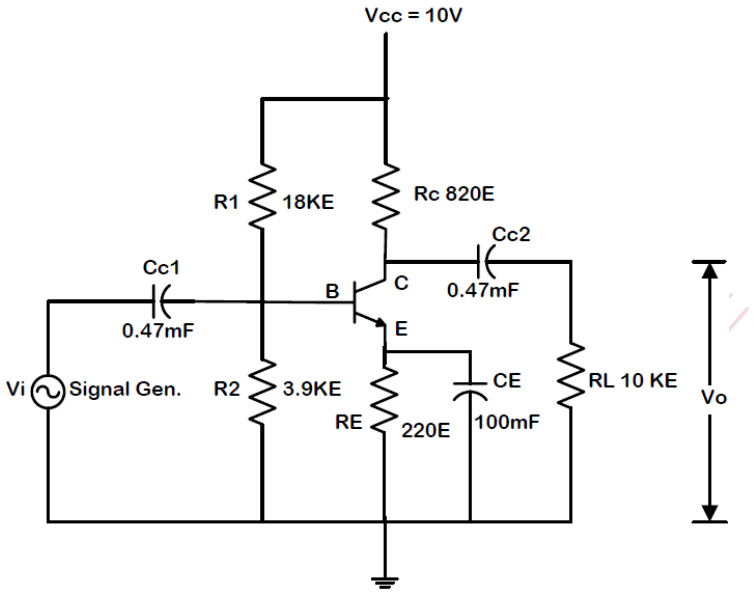
Also use $C_{C1} = C_{C2} = 0.47\ \mu F$

Procedure:

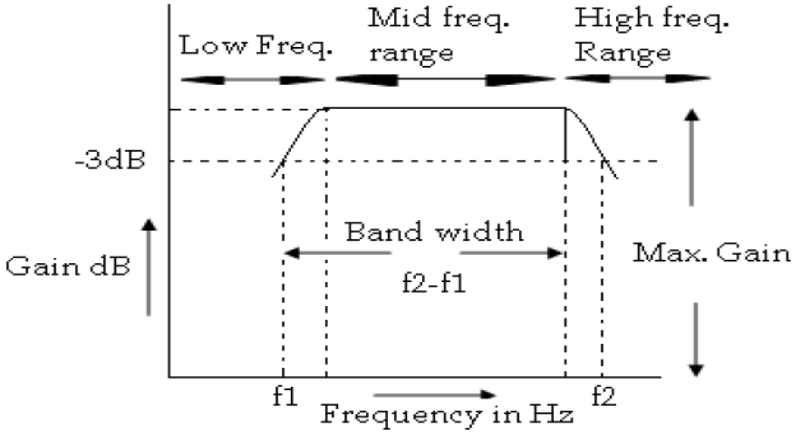
- Rig up the circuit
- Apply the sinusoidal input of 50m(P-P) and observe the input and output waveforms simultaneously on the CRO screen
- By varying the frequency of the input from Hz to maximum value and note down the output voltages

- Plot the frequency response (gain in dB vs log f) and determine the bandwidth from the graph

Circuit Diagram:



Waveforms:



Tabular Column:

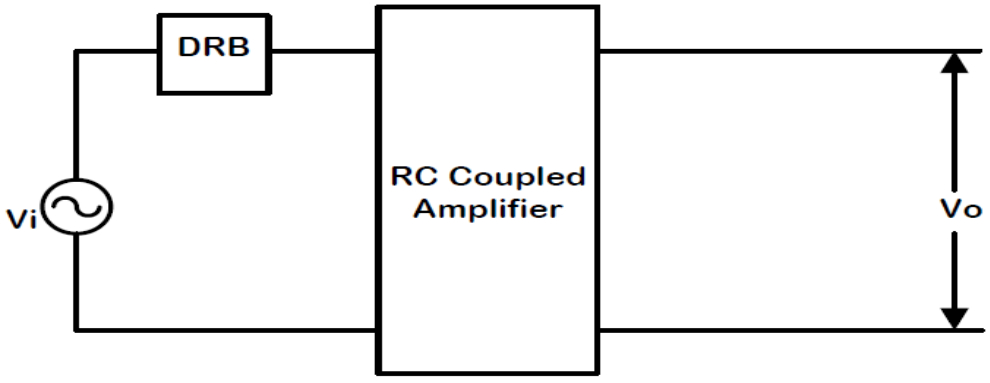
Freq. in Hz	$V_{o\ P\text{-}P}$	$A_V = {}^{Vo}/_{V1}$	Gain in dB $= 20 \log_{10} A_V$
50 Hz 100 Hz 200 Hz 300 Hz 500 Hz 1KHz			

To measure input impedance and output impedance:

I) Input impedance (Ri):

Procedure:

- Connect the circuit as shown
- Set the DRB to a minimum value
- Set the output to a convenient level and note down the output voltage
- Increase the DRB value till VO becomes half of the maximum amplitude
- The corresponding DRB value gives input impedance

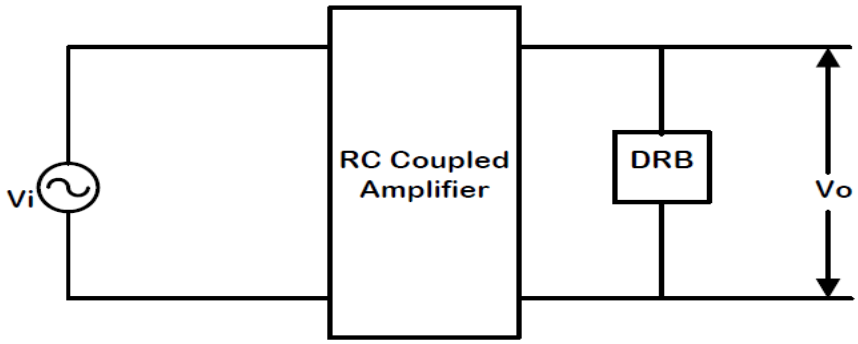


II) Output impedance (RO):

Procedure:

- Connect the circuit as shown
- Set the DRB to a maximum value
- Set the output to a convenient level and note down the output voltage
- Increase the DRB value till VO becomes half of the maximum amplitude

- The corresponding DRB value gives input impedance



RESULT:

EXPERIMENT NO : 2

R.C.PHASE SHIFT OSCILLATOR

Aim: To design and test the RC Phase shift Oscillator for the frequency of 1KHz.

Components required:

-Transistor (BC 107)

- Resistors

- CRO

- Capacitors

- Connecting wires

- Bread board

- Power supply

Design:

$V_{CC} = 12V$

$I_C = 2mA$

$V_{RC} = 40\%\ V_{CC} = 4.8V$

$V_{RE} = 10\%\ V_{CC} = 1.2V$

$V_{CE} = 50\%\ V_{CC} = 6V$

To find R_C, R_1, R_E & R_2

We Have,

$V_{RC} = I_C R_C = 4.8V$

$R_C = 2.4K\Omega$

Choose $R_C = 2.2K\Omega$

$V_{RE} = I_E R_E = 1.2V$

$R_E = 600\Omega$

Choose $R_E = 680\Omega$

$h_{fe} = 100$ (For BC 107)

$I_B = \frac{I_C}{h_{fe}} = 20mA$

Assume current through $R_1 = 10\ I_B$ & through $R_2 = 9\ I_B$

$VR_1 = V_{CC} - V_{R2}$

$= 10V$

Also, $VR_1 = 10\ I_B\ R_1 = 10.1V$

R_1= 50KΩ

Choose R_1= 47KΩ

$VR_2 = V_{BE+}V_{RE}$

= 0.7+1.2

= 1.9V

Also, VR_2 =9 I_B R_2=1.9V

R_2= 10.6KΩ

Choose R_1= 12KΩ

To find C_C & C_E

$$X_{CE} = \frac{1}{2\pi C_E} = \frac{1}{10} R_E = \frac{680}{10} = 68\Omega$$

For ϑ = 20Hz

C_E= 117μF

Choose C_E = 220 μF

$$X_{CC} = \frac{1}{2\pi C_C} = \frac{R_C}{10} = 220\Omega$$

For ϑ = 20Hz

Choose C_C = 47 μF

Design of ϑ Selective Circuit:

Required ϑ of oscillations f = 1KHz

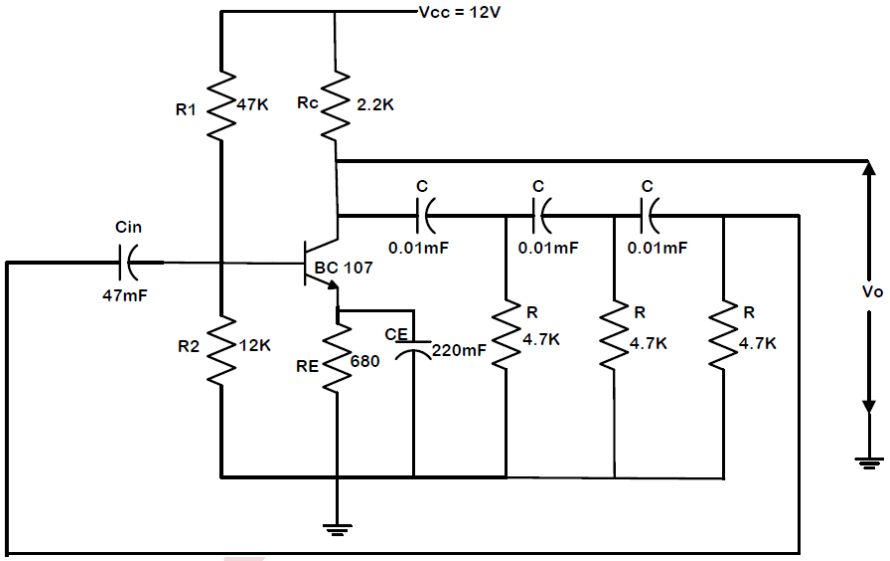
$$f = \frac{1}{2\pi R_{C\sqrt{6}+\frac{4R_C}{R}}}$$

Take R= 4.7KΩ & C=0.01μF

Procedure:

- Rig up the circuit as shown in the figure
- Observe the sinusoidal output voltage.
- Measure the frequency and compare with the theoretical values.

Circuit Diagram:



RESULT:

EXPERIMENT NO : 3

MEASUREMENT OF OP AMP PARAMETERS

AIM:

To measure the following parameters of an Op-amp i.e, input bias current, input offset voltage, input offset current, CMRR and slew rate.

APPARATUS REQUIRED:

The following components and equipments are used to measure the op-amp parameters

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	±15 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	4.7KΩ,100KΩ(2), 1MΩ, 100Ω(2),	Each one
5	Capacitor	0.01μF	1
6	Op-amp	IC 741	1
8	Bread board	-	1
9	Connecting wires	-	As required

PRINCIPLE & PROCEDURE:

Input bias current I_B: It is defined as the average of the currents entering into the inverting and non-inverting terminals of an op-amp. $I_B = (I_{B1}+I_{B2})/2$. Typical value of input bias current is 80nA.

Input bias current I_O: It is defined as the algebraic difference between the currents entering into the inverting and non-inverting terminals of an op-amp. $I_O=|I_{B1}+I_{B2}|$. Typical value of input offset current is 20nA.

Input offset voltage: It is defined as the small voltage which is applied to overcome circuit imbalances due to which the output voltage is not zero for zero input voltage, i.e., voltage applied between the input terminals of an op-amp to nullify the output voltage. Typical value of input offset voltage is 2mV.

CMRR: It is the ratio of differential mode gain to common mode gain and is expressed in dB. CMRR=20 log (A_d/A_c) in dB.

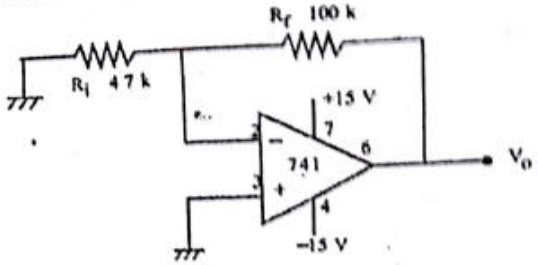
Slew rate: It is the rate of rise of output voltage. It is a measure of fastness of op-amp. It is expressed in v/μs.

PROCEDURE:

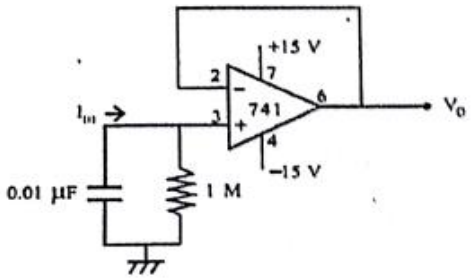
1. Set up the circuit to find the input offset voltage.
2. Measure the output voltage using the expression, $V_{iO}=V_O R_i/(R_f + R_i)$; where V_O is the output voltage and V_{iO} is the input offset voltage.

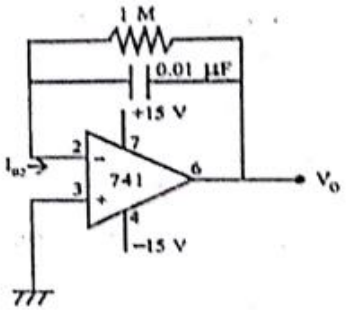
Circuit diagram

To measure input offset voltage

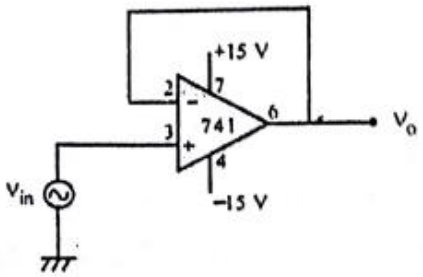


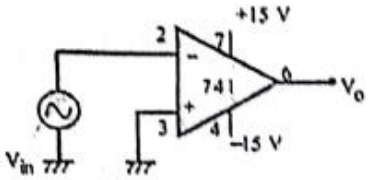
To measure input bias and input offset currents



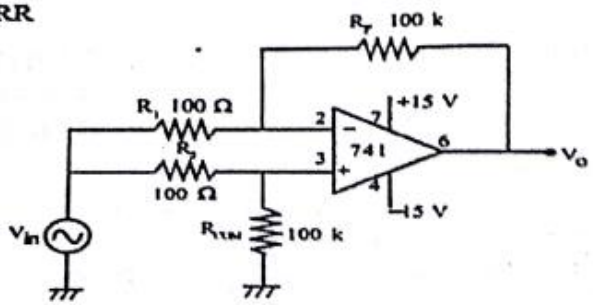


To measure slew rate





CMRR



3. Set up the circuits for measuring input bias current and input bias voltage
4. Measure the output voltage using the expressions $V_O = I_{b1}R$ and $V_O = I_{b2}R$.
5. Calculate I_{B1} and I_{B2} and measure the bias and offset currents using the expression $I_B = (I_{B1}+I_{B2})/2$and $I_O = |I_{B1} - I_{B2}|$. Where I_B is bias current, I_O is offset current.
6. Setup the circuit to calculate the slew rate. Give a square input of 1 V_{pp}, 1kHz. Vary the input frequency and observe the output. Note down the frequency at which the output gets disturbed. Calculate the slew rate using the expression $SR = (2\pi f V_m)/10^6$
7. Set up the circuits for finding CMRR and apply a dc signal of 0.5v to input and measure V_O. Calculate the CMRR using the expression $CMRR = V_i(R_f/R_i)/V_O$. Express the CMRR in dB using the expression 20 log(CMRR).

RESULT:

INFERENCE:

EXPERIMENT 4

INVERTING, NON INVERTING AMPLIFIER AND VOLTAGE FOLLOWER

AIM

To study the following op-amp circuits

1. Inverting amplifier
2. Non-inverting amplifier

DESIGN

1. Design for inverting amplifier

The expression for gain is $A_{CL} = -\left(\frac{R_f}{R_1}\right)$

Let amplifier to be designed with a gain of (-10), select input resistance R_1=10kΩ

Feedback resistance, $R_f = -(A_{CL} \times R_1)$

$= -(-10 \times 10 \times 10^3) = 100\ k\Omega$

2. Design for non- inverting amplifier

The expression for gain is $A_{CL} = \left(1 + \frac{R_f}{R_1}\right)$

Let amplifier to be designed with a gain 11 and select $R_1 = 10\text{k}\Omega$

Feedback resistance, $Rf = (A_{CL} - 1)R_1$

$= (10-1) \times 10 \times 10^3 = 100\ k\Omega$

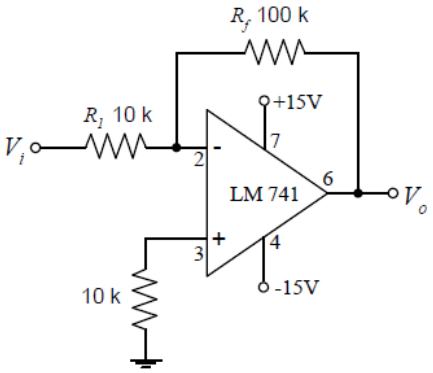


Fig 1. Circuit diagram of inverting amplifier

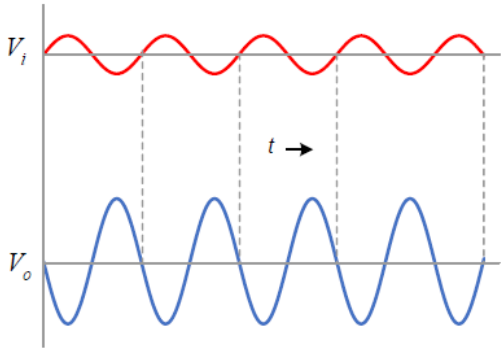


Fig 2. Input and output waveforms of inverting amplifier

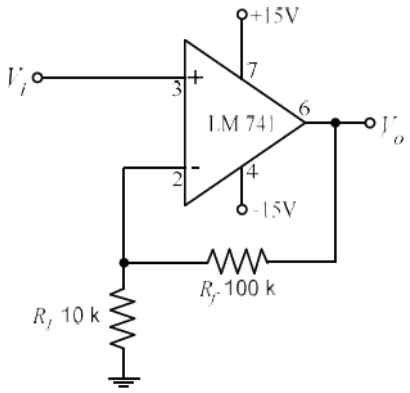


Fig 3. Circuit diagram of non-inverting amplifier

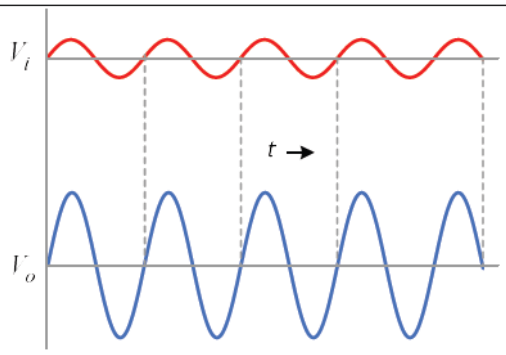


Fig 4. Input and output waveforms of non-inverting amplifier

PROCEDURE

1. Inverting Amplifier

   Set up the circuit as shown in Fig 1. The circuit gives a closed loop gain $A_{CL} = -\left(\frac{R_f}{R_1}\right)$. This gain is very small compared to the open loop gain of the op-amp. Test the circuit by applying the input signal of suitable amplitude (say 1V peak to peak) from a function generator. Observe the output waveform on the CRO and determine actual gain.

2. Non-inverting Amplifier:

   The circuit of a non-inverting amplifier is shown in Fig 3. Its closed loop gain is $A_{CL} = \left(1 + \frac{R_f}{R_1}\right)$. The circuit is tested by applying the input signal of suitable amplitude (say 1V peak to peak) from a function generator. Observe the output waveform on the CRO and determine actual gain.

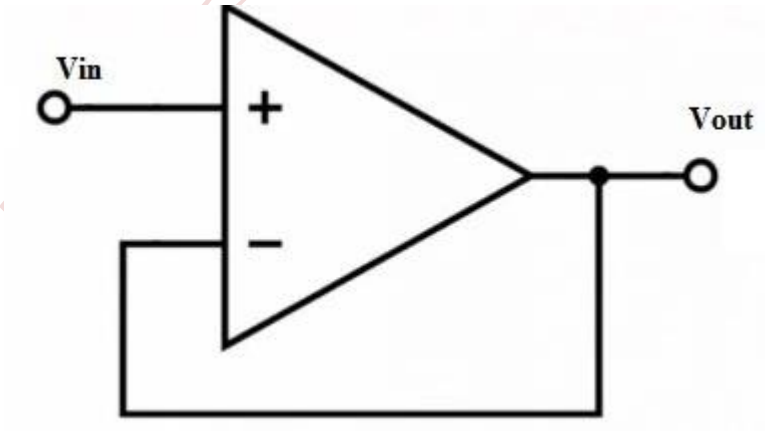
OBSERVATIONS

Inverting Amplifier

Input Frequency F kHz	Input voltage (p-p) V_i V	Output voltage (p-p) V_o V	Gain $A_{CL} = \frac{V_o}{V_i}$

Non-inverting Amplifier

Input Frequency f kHz	Input voltage (p-p) V_i V	Output voltage (p-p) V_o V	Gain $A_{CL} = \frac{V_o}{V_i}$



Circuit : Voltage follower

RESULT

EXPERIMENT 5

INTEGRATOR, DIFFERENTIATOR & SCHMITT TRIGGER

AIM:

To design and set up integrator and differentiator circuits using op-amp and plot their frequency responses.

APPARATUS REQUIRED:

The following components and equipments are used to design and set up integrator and differentiator

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	15 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	150KΩ, 15KΩ(2), 5.6KΩ(2)	Each one
5	Capacitors	0.01uf, 0.1uf(2)	1
6	Op-amp	IC 741	1
7	Bread board	-	1
8	Connecting wires	-	As required

PRINCIPLE & PROCEDURE:

Integrator: In an integrator circuit, the output voltage is integral of the input signal. The output voltage of an integrator is given by

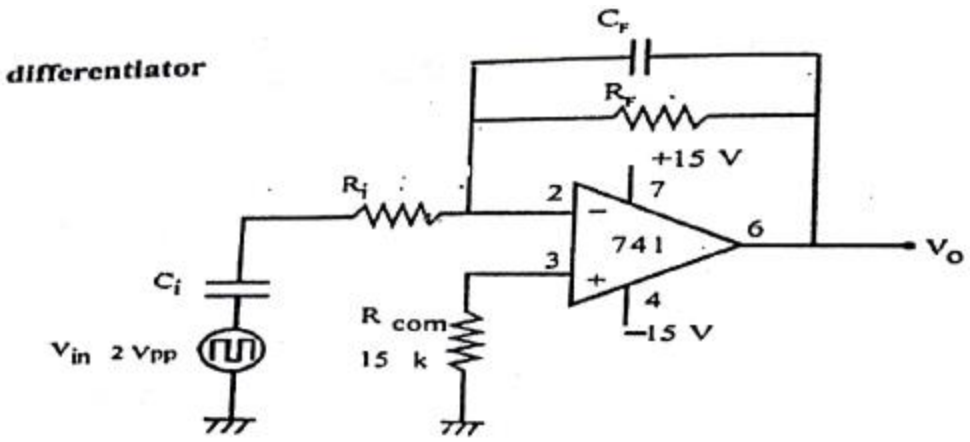
$$V_o = -1/R_1C_f \int_o^t Vidt$$

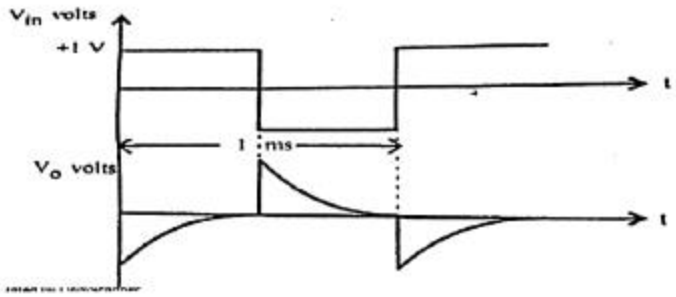
At low frequencies the gain becomes infinite, so the capacitor is fully charged and behaves like an open circuit. The gain of an integrator at low frequency can be limited by connecting a resistor in shunt with capacitor.

Differentiator: In the differentiator circuit the output voltage is the differentiation of the input voltage. The output voltage of a differentiator is given by

$$V_o = -RfC_1 \frac{dV_i}{dt}$$

The input impedance of this circuit decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise. At high frequencies circuit may become unstable.





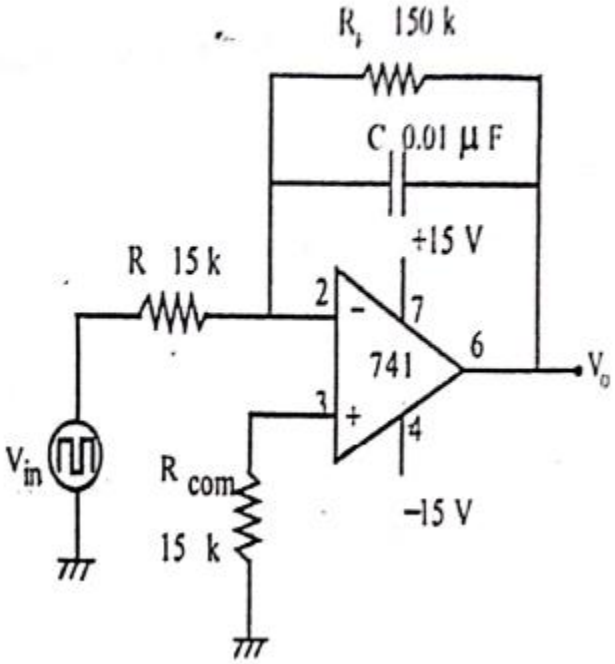
DESIGN:

INTEGRATOR:
Let input frequency be ,f= 1 kHz
$f = 1/ (2\pi RC)$
Take C=0.01 µf. Then R=15.9. Use 15k std.
Select $R_f = 10\ R = 10 * 15\ k = 150\ k$ so that break frequency is 100 Hz.
Select $R_{com} = 15k$

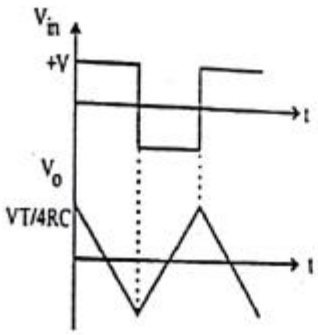
DIFFERENTIATOR:
Frequency at which gain become zero dB $f_a = 1/(2\pi R_f C_f) = 1$ kHz
Let C_f=0.01uF, Then R_f=15.9k. Use 15k std.
Let Gain limiting frequency, $f_b = 1/(2\pi R_f C_f) = 10 f_a = 10$kHz
Take C_i =0.01uF, Then R_i=1.59k. Use 1.5k std.
Select $R_{com} = 15k$

CIRCUIT DIAGRAM

INTEGRATOR



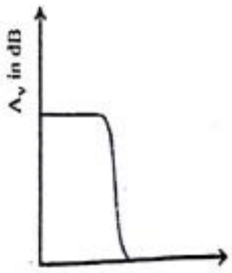
Waveforms



Tabular column

f in Hz	V_o	log (f)	A_v in dB

Frequency response



PROCEDURE:

INTEGRATOR:

1. Set up the integrator circuit.
2. Feed 1V, 1ms square wave at the input and observe the input and output simultaneously on CRO.
3. Feed a sine wave to the input and note down the output amplitude by varying the frequency of the sine wave. Enter it in tabular column and plot the frequency response.

DIFFERENTIATOR:

1. Set up the differentiator circuit.
2. Feed 1V, 1ms square wave at the input and observe the input and output simultaneously on CRO.
3. Feed a sine wave to the input and note down the output amplitude by varying the frequency of the sine wave. Enter it in tabular column and plot the frequency response

RESULT:

INFERENCE:

EXPERIMENT 6

ASTABLE MULTIVIBRATOR USING IC 555

AIM

To design and set up astable multivibrator of 1000 Hz frequency and 60% duty cycle using IC 555

THEORY

IC 555 timer is an analog IC used for generating accurate time delay or oscillations. The entire circuit is usually housed in an 8-pin package as specified in figures 1 & 2 below. A series connection of three resistors inside the IC sets the reference voltage levels to the two comparators at $\frac{2}{3}V_{CC}$ and $\frac{1}{3}V_{CC}$, the output of these comparators setting or resetting the flip-flop unit. The output of the flip-flop circuit is then brought out through an output buffer stage. In the stable state the $\bar{Q}$ output of the flip-flop is high (ie Q low). This makes the output (pin 3) low because of the buffer which basically is an inverter.The flip-flop circuit also operates a transistor inside the IC, the transistor collector usually being driven low to discharge a timing capacitor connected at pin 7. The description of each pin s described below,

Pin 1: (Ground): Supply ground is connected to this pin.

Pin 2: (Trigger): This pin is used to give the trigger input in monostable multivibrator. When trigger of amplitude greater than (1/3)Vcc is applied to this terminal circuit switches to quasi-stable state.

Pin 3: (Output)

Pin 4 (Reset): This pin is used to reset the output irrespective of input. A logic low at this pin will reset output. For normal operation pin 4 is connected to Vcc.

Pin 5 (Control): Voltage applied to this terminal will control the instant at which the comparator switches, hence the pulse width of the output. When this pin is not used it is bypassed to ground using a 0.01μF capacitor.

Pin 6 (Threshold): If the voltage applied to threshold terminal is greater than (2/3)V_{CC}, upper comparator switches to +Vsat and flip-flop gets reset.

Pin 7: (Discharge): When the output is low, the external capacitor is discharged through this pin

Pin 8 (V_{CC}): The power supply pin

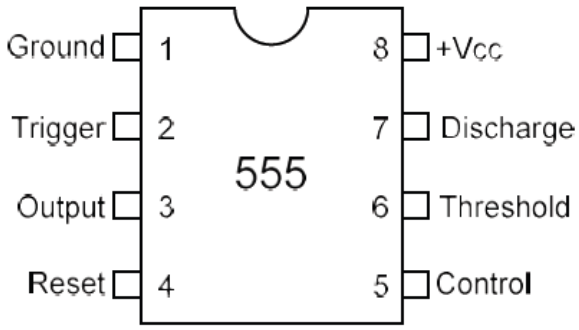


Figure 2: IC 555 pin diagram

Astable multivibrator using IC 555

One popular application of the 555 timer IC is as an astable multivibrator or clock Circuit. Figure 3 shows an astable circuit built using 2 external resistors and a capacitor to set the timing interval of the output signal. Capacitor C charges toward V_{CC} through external resistors R_A and R_B. Referring to figure, the capacitor voltage rises until it goes above $\frac{2}{3}V_{CC}$. This voltage is the threshold voltage at pin 6, which drives comparator 1 to trigger the flip-flop(Q low $\bar{Q}$ high) so that the output at pin 3 goes low. In addition, the discharge transistor is driven on, causing the output at pin 7 to discharge the capacitor through resistor R_B. The capacitor voltage then decreases until it drops below the trigger level $\frac{1}{3}V_{CC}$. The flipflop is triggered so that the output goes back high and the discharge transistor is turned off, so that the capacitor can again charge through resistors R_A and R_B towards V_{CC}.

CIRCUIT DIAGRAM & DESIGN

Take $V_{CC} = 10V$ and $f = 1000$ Hz and duty cycle = 60 %

Then $t = 1$ ms, $t_H = 0.6$ ms, $t_L = 0.4$ ms

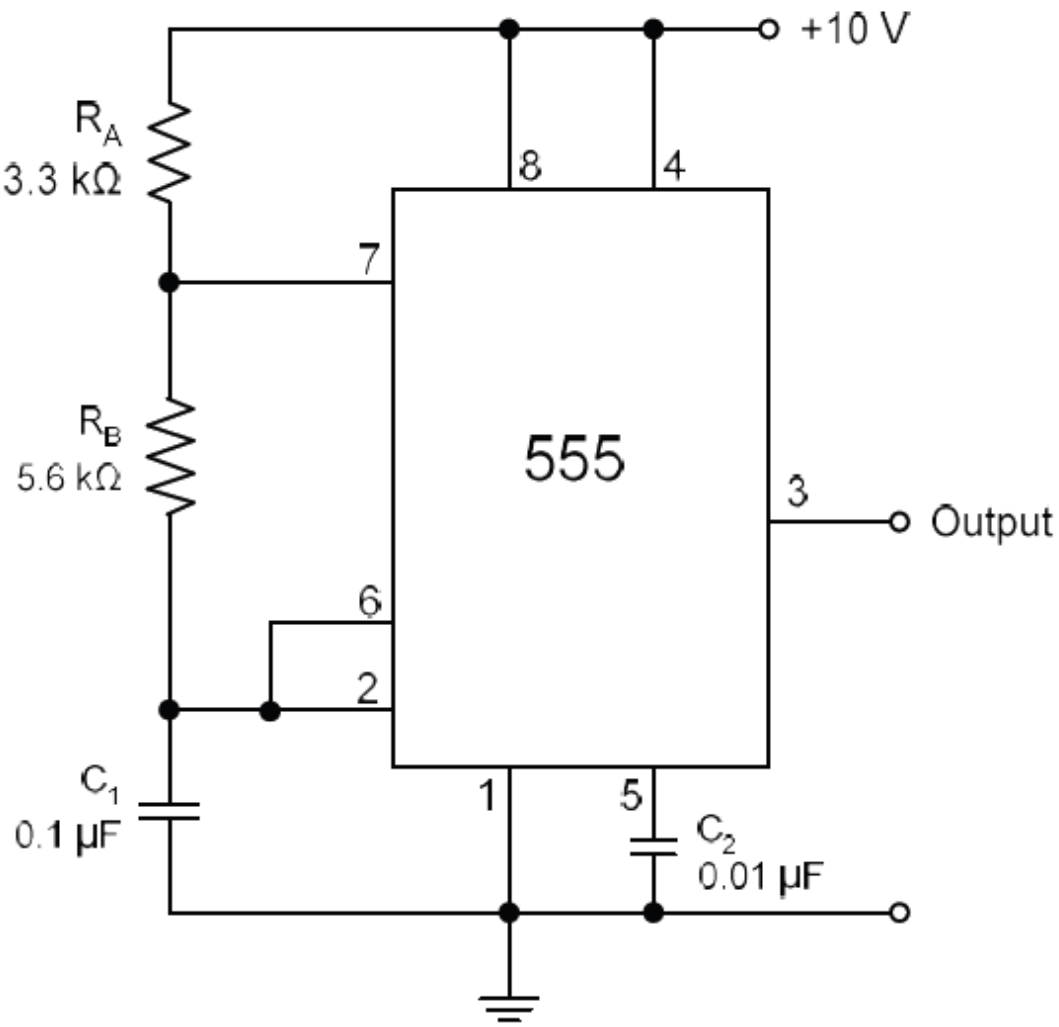


Figure 3 Astable multivibrator circuit using IC 555

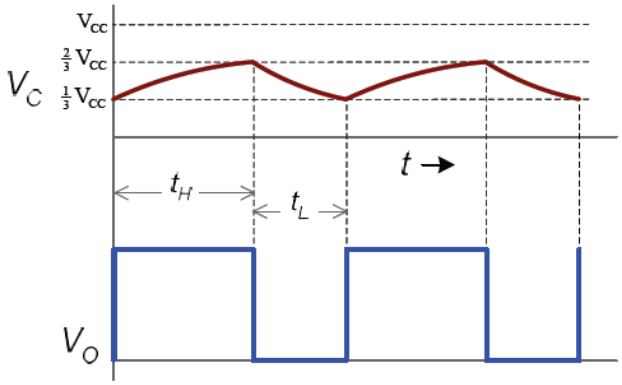


Figure 4 Waveforms of voltage across the capacitor and output voltage

Assume C = 0.1 μF

$t_L = 0.693 \times R_B \times C$ then $R_B = 5.77$ kΩ take $R_B = 5.6$ kΩ

$t_H = 0.693 \times (R_A + R_B) \times C$ then $R_A = 3.06$ kΩ take $R_A = 3.3$ kΩ

The resistance R_A and R_B should be in the range of 1k to 10k to limit the collector current of the internal transistor.

PROCEDURE

1. Set up the circuit after verifying the condition of IC
2. Observe the waveforms at pin number 3 and 6 of the IC

RESULT

Astable multivibrator using timer IC 555 is designed and setup, and the waveforms are obtained.

Design of Monostable Multivibrator Circuit using 555 Timer:

AIM: To construct and study the operation of a monostable multivibrator using 555 IC timer.

APPARATUS:

S.NO.	Name of the Equipment	Values	Quantity
1	555 IC Timer		1
2	Resistor	10 KΩ	1
3	Capacitors	10nF, 0.1μF, 0.01μF	1
4	Function Generator	1MHz	1
5	CRO	20 MHz	1
6	Bread Board		1
7	Connecting Wires and Probes		

THEORY:

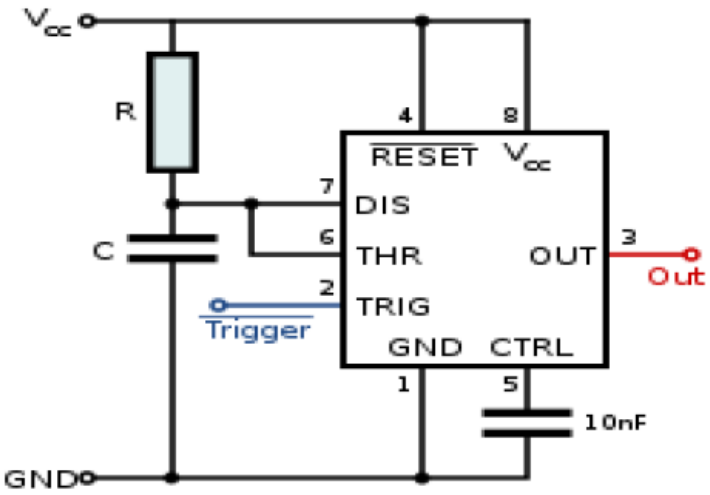
It has one stable and one quasi stable state. The circuit is useful for generating single output pulse of time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. The diode gives a negative triggering pulse. When the output is +Vsat, a diode clamps the capacitor voltage to 0.7V then, a negative going triggering impulse magnitude Vi passing through RC and the negative triggering pulse is applied to the positive terminal. Let us assume that the circuit is instable state. The output V0i is at +Vsat. The diode D1 conducts and Vc the voltage across the capacitor 'C' gets clamped to 0.7V,the voltage at the positive input terminal through R1R2 potentiometer divider is +ßVsat. Now, if a negative trigger of magnitude Vi is applied to the positive terminal so that the effective signal is less than 0.7V.the output of the Op-Amp will switch from +Vsat to –Vsat. The diode will now get reverse biased and the capacitor starts charging exponentially to –Vsat. When the capacitor charge Vc becomes slightly more negative than –ßVsat, the output of the op-amp switches back to +Vsat. The capacitor 'C' now starts charging to +Vsat through R until Vc is 0.7V.

$V_0 = V_f + (V_i - V_f)\, e^{t/RC}$, ß = R2/(R1+R2)

If Vsat >> Vp and R1=R2 and ß = 0.5,

Then, T = 0.69RC

Circuit Diagram:



Procedure:

1. Connect the circuit as shown in the circuit diagram.
2. Apply Negative triggering pulses at pin 2 of frequency 1 KHz as shown in Fig.
3. Observe the output waveform and capacitor voltage as shown in Figure and measure the pulse duration.
4. Theoretically calculate the pulse duration as $T_{high} = 1.1\ RC$
5. Compare it with experimental values.

Result:

EXPERIMENT 7

STUDY THE RESPONSE OF ACTIVE FIRST ORDER LPF & HPF

AIM

To study the response of active first order LPF & HPF

APPARATUS REQUIRED:

S.NO	APPARATUS	SPECIFICATION	QUANTITY
1	SIGNAL GENERATOR	(0-10)mHz	1
2	Op amp	IC741	3
3	Resistors	1kΩ,1.5kΩ 5kΩ,10kΩ	2,1,2,4
4	Capacitor	0.1μf	4
5	linear power supply	±15V	1
6	DSO	-	1

THEORY:

Electronic filters are circuits which perform signal processing functions, specifically to remove unwanted frequency components from the signal, to enhance wanted ones, or both. Electronic filter high-pass, low-pass, band-pass, band-stop (band-rejection; notch), or all-pass.

Active Low Pass Filter:

The most common and easily understood active filter is the **Active Low Pass Filter**. Its principle of operation and frequency response is exactly the same as those for the previously seen passive filter, the only difference this time is that it uses an op-amp for amplification and gain control. The simplest form of a low pass active filter is to connect an inverting or non-inverting amplifier.

High Pass Filter :

A first-order (single-pole) **Active High Pass Filter** as its name implies, attenuates low frequencies and passes high frequency signals. It consists simply of a passive filter section followed by a non-inverting operational amplifier. The frequency response of the circuit is the same as that of the passive filter, except that the amplitude of the signal is increased by the gain of the amplifier and for a non-inverting amplifier the value of the pass band voltage gain is given as 1 + R2/R1, the same as for the low pass filter circuit.

Procedure:

1)Connect the circuit as shown in diagram.

2)Connect the DSO to the probes and switch it on.

3)Check the graph for both positive and negative voltage and write down the outut.

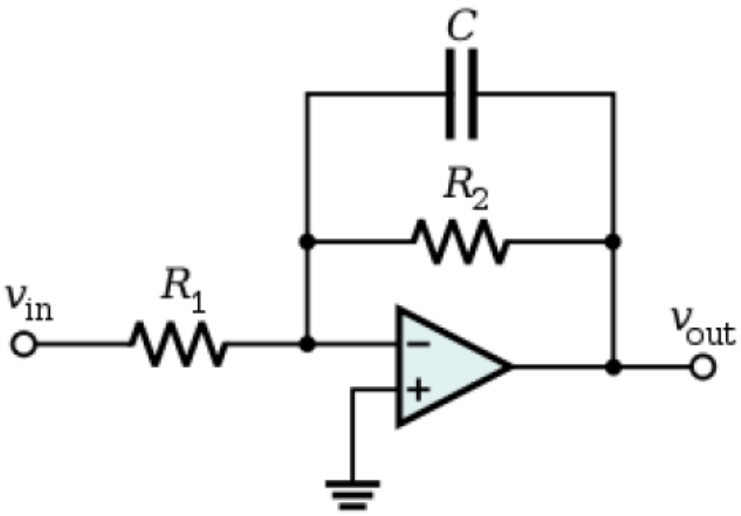
DESIGN CALCULATION:

$$fc = \frac{1}{2\pi RC} \; or \; \frac{1}{2\pi\tau}$$

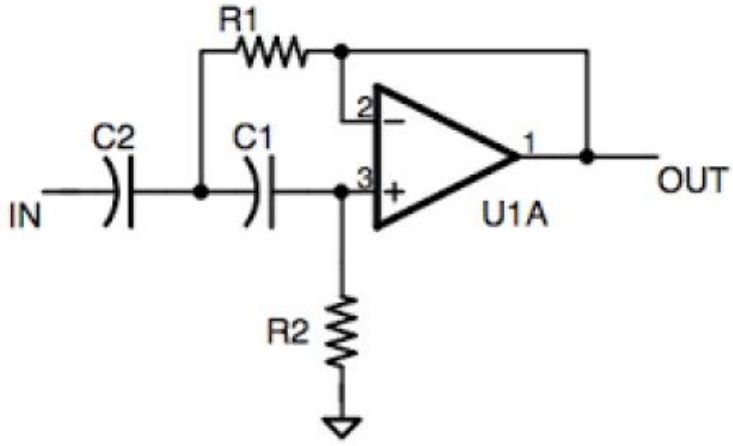
$$GAIN = (1 + \frac{Rf}{Ri})$$

CIRCUIT DIAGRAM:

LOW PASS FILTER:



HIGH PASS FILTER:



low pass filter:

High pass filter:

TABULATION:

LPF:

INPUT FREQUENCY(HZ)	OUTPUT VOLTAGE(V)	GAIN	GAIN IN dB

HPF:

INPUT FREQUENCY(HZ)	OUTPUT VOLTAGE(V)	GAIN	GAIN IN dB

RESULT

EXPERIMENT 8

FAMILIARIZATION OF LOGIC GATES

AIM

To familiarize with the standard logic gates and to verify their truth tables.

COMPONENTS AND EQUIPMENTS REQUIRED

IC-7400, IC-7402, IC-7404, IC-7432, IC-7408, IC-7486, Logic probe & IC trainer kit

THEORY

In digital electronics, a gate is a logic circuit with one output and one or more inputs. Logic gates are available as integrated circuits (IC's).

AND GATE

The AND gate performs logical multiplication, more commonly known as AND operation. The AND gate out put will be in high state only when all the inputs are in high state.IC-7408 is a quad 2 input AND gate.

OR GATE

It performs logical addition. Its output will become high if any of the inputs are in logic high. IC-7432 is a quad two input OR gate.

NOT GATE

It performs a basic logic function called inversion or complementation. The purpose of the inverter is to change one logic level to opposite level. IC- 7404 is a hex inverter.

NAND GATE

A NOT gate following an AND gate is called NOT-AND gate or NAND gate. Its output will be low if all the inputs are in the high state.IC-7400 is a quad 2 input NAND gate.

NOR GATE

A not gate following an OR gate is called NOT-OR gate. Itsout put will be in low state if any of its inputs is in high state. 7402 is quad two input NOR gate.

X-OR Gate

Its output will be high if one input is in high state. 7486 is a quad two inputs X-OR gate.

SR FLIP FLOP

The SR flip flop is a 1-bit memory bistable device having two inputs, i.e., SET and RESET. The SET input 'S' set the device or produce the output 1, and the RESET input 'R' reset the device or produce the output 0. The SET and RESET inputs are labeled as **S** and **R**, respectively

T FLIP FLOP

In T flip flop, "T" defines the term "Toggle". In SR Flip Flop, we provide only a single input called "Toggle" or "Trigger" input to avoid an intermediate state occurrence. Now, this flip-flop work as a Toggle switch. The next output state is changed with the complement of the present state output. This process is known as "Toggling'".

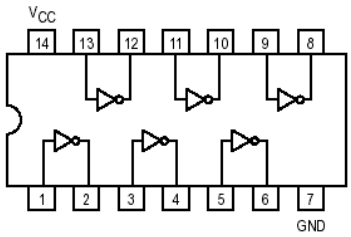
D FLIP FLOP

The D flip flop is the most important flip flop from other clocked types. It ensures that at the same time, both the inputs, i.e., S and R, are never equal to 1. The Delay flip-flop is designed using a gated SR flip-flop with an inverter connected between the inputs allowing for a single input D(Data).

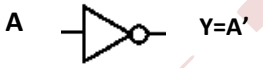
JK FLIP FLOP

The JK flip flop work in the same way as the SR flip flop work. The JK flip flop has 'J' and 'K' flip flop instead of 'S' and 'R'. The only difference between JK flip flop and SR flip flop is that when both inputs of SR flip flop is set to 1, the circuit produces the invalid states as outputs, but in case of JK flip flop, there are no invalid states even if both 'J' and 'K' flip flops are set to 1.

NOT GATE IC- 7404



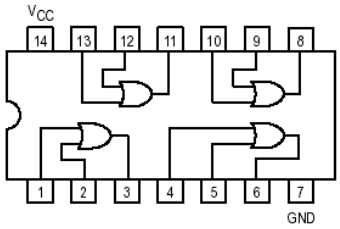
LOGIC DIAGRAM

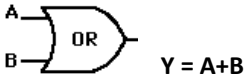


TRUTH TABLE

A	Y
0	1
1	0

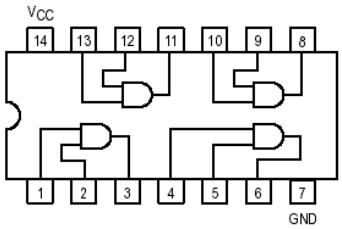
OR GATE IC-7432

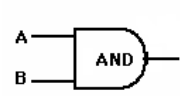




Inputs		Outputs
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

AND GATE IC-7408

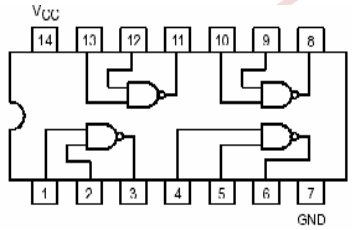


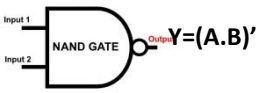


Y = A.B

Inputs		Outputs
A	**B**	**Y**
0	0	0
0	1	0
1	0	0
1	1	1

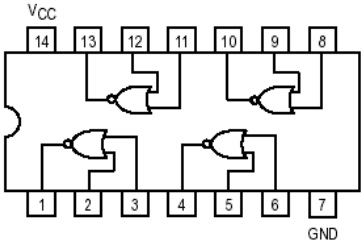
NAND GATE IC-7400

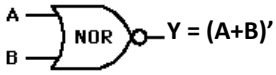




Inputs		Outputs
A	**B**	**Y**
0	0	1
0	1	1
1	0	1
1	1	0

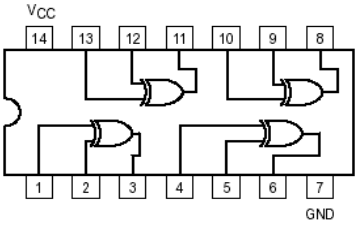
NOR GATE IC 7402

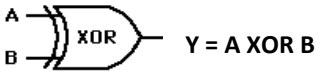




Inputs		Outputs
A	**B**	**Y**
0	0	1
0	1	0
1	0	0
1	1	0

XOR GATE IC 7486

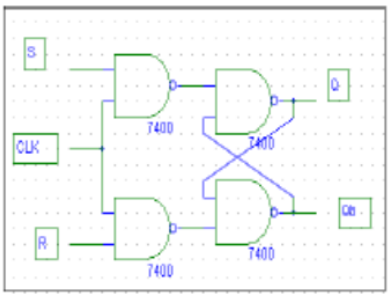




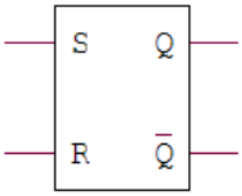
Inputs		Outputs
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	0

SR FLIP FLOP

CIRCUIT DIAGRAM:



(A) LOGIC DIAGRAM



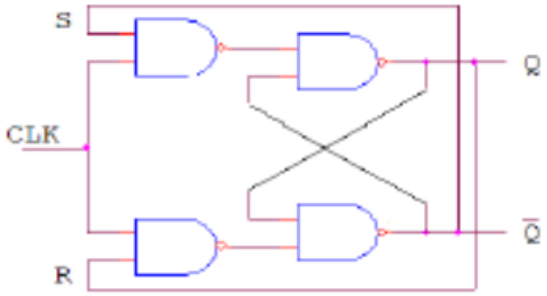
(B) SYMBOL

TRUTH TABLE

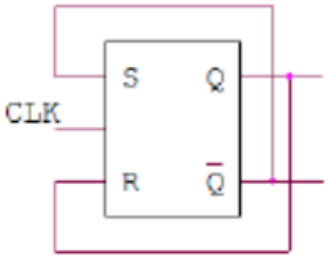
S	R	Q+	$\overline{Q}$b+
0	0	Q	$\overline{Q}$b
0	1	0	1
1	0	1	0
1	1	0*	0*

T FLIPFLOP

LOGIC DIAGRAM



SYMBOL

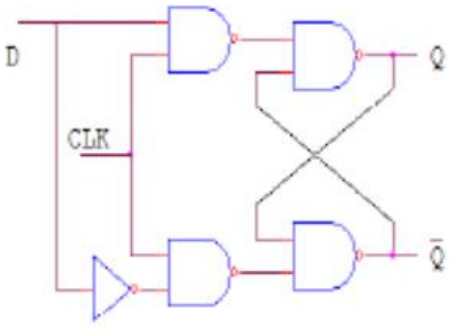


TRUTH TABLE

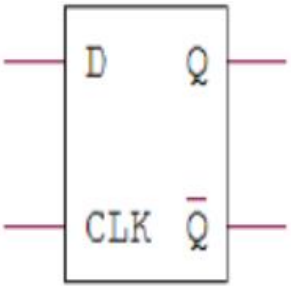
T	Qn + 1
0	Qn
1	$\overline{Qn}$

D FLIP FLOP

LOGIC DIAGRAM



SYMBOL

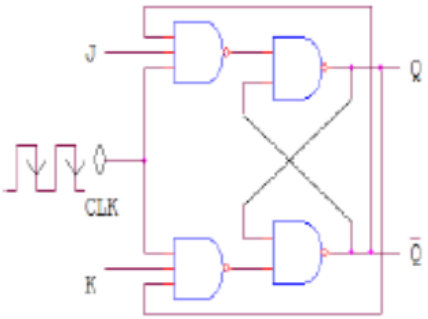


TRUTH TABLE

CLOCK	D	Q+	$\overline{Q+}$
0	X	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

JK FLIP FLOP

LOGIC DIAGRAM



TRUTH TABLE

Clock	J	K	Q+	Q'+	Comment
1	0	0	Q	Q'	No Change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	Q'	Q	Toggle

TRUTH TABLE

SD	RD	Clock	J	K	Q	Q'	Comment
0	0	Not Allowed					
0	1	X	X	X	1	0	Set
1	0	X	X	X	0	1	Reset
1	1	1	0	0	NC	NC	Memory
1	1	1	0	1	0	1	Reset
1	1	1	1	0	1	0	Set
1	1	1	1	1	Q'	Q	Toggle

TROUBLE SHOOTING WITH DIGITAL ICs

Experiments with digital integrated circuits are rather easy compared with analog integrated circuits. Operator must be careful about the connecting wires and pins of the IC. In most of the logic gate IC s, pin no 7 is GND and pin no 14 is V_{CC} . But this is not the case with all digital ICs. There is a chance that the operator committing a mistake by taking for granted that pin no 7 and 14 are GND and VCC respectively for all 14 pin ICs.

PROCEDURE

Test all the components and IC packages using a digital IC tester.

Also assure whether all the connecting wires were in good condition by testing for the continuity using a multi meter or a trainer kit.

Continuity of wire can be tested using a trainer kit by shorting a 5 V supply in the trainer to an LED of the panel. If the wires are good, LED will glow.

Verify the dual in line package (DIP) pin out of the IC before feeding the inputs.

Setup the circuits and observe the outputs. Enter the inputs and output states in the truth table corresponding to the input combinations

RESULT

EXPERIMENT 9

DESIGN AND IMPLEMENTATION OF FULL ADDER AND SUBTRACTOR

AIM

To implement the full adder and full subtractor circuit and verify their truth tables.

COMPONENTS AND EQUIPMENTS REQUIRED

IC-7486, IC-7404, IC-7432, IC-7408, Logic probe & IC Trainer kit.

THEORY

FULL ADDER

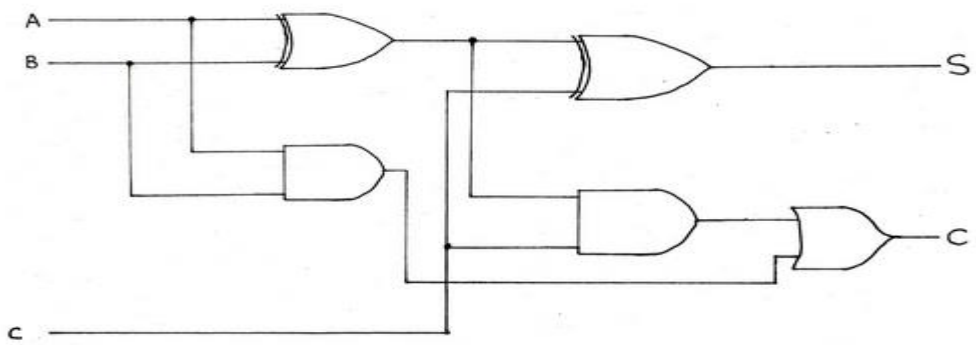
A full adder circuit is central to most digital circuits that perform addition or subtraction. It is so called because it adds together two binary digits, plus a carry-in digit to produce a sum and carry-out digit.1 It therefore has three inputs and two outputs.

TRUTH TABLE OF FULL ADDER

A	B	C_{n-1}	S	C
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

K-MAP FOR FULL ADDER

FULL ADDER USING BASIC GATES



FULL SUBTRATOR

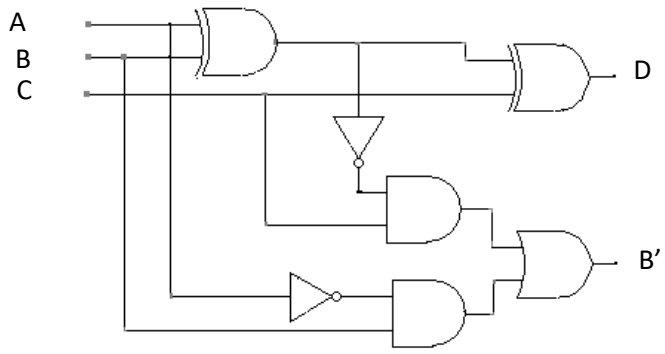
A full subtractor is a combinational circuit that performs subtraction of two bits, one is minuend and other is subtrahend, taking into account borrow of the previous adjacent lower minuend bit. This circuit has three inputs and two outputs. The three inputs A, B and Bin, denote the minuend, subtrahend, and previous borrow, respectively. The two outputs, D and Bout represent the difference and output borrow, respectively.

TRUTH TABLE OF FULL SUBTRACTOR

A	B	C	D	B′
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

K-MAP FOR FULL SUBTRACTOR

FULL SUBTACTOR USING BASIC GATES



PROCEDURE

1. Verify whether all the components and wires are in good condition.
2. Setup the adder and subtractor circuit and feed the input combinations.
3. Observe the output corresponding input combinations and enter it in the truth table.

RESULT

EXPERIMENT 10

I. BINARY TO GRAY AND GRAY TO BINARY CONVERTERS

AIM

To design and setup following circuits :

A 4-bit binary to gray code converter & A 4-bit gray to binary code converter

COMPONENTS AND EQUIPMENTS REQUIRED

IC's 7486, 7408 and IC trainer kit

THEORY

Binary to gray code converter

It apply the following rules :

1. The MSB in the gray code is same as the corresponding bit in a Binary number
2. Going from left to right, add each adjacent pair of binary digits to get the next Gray code digit .Discard carries.

Gray to binary code converter

Gray code is also called mirror image code. To covert Gray code to binary code, following rules are to be observed.

1. The MSB in the binary is same as that in gray code.
2. From left to right add binary digit generated already to the gray code in next position to get the next binary digit .Discard the carry.

To design these converters obtain the truth table and get the simplified expression using K maps for each binary digit as the function of gray code digit and vice versa.

4-bit Binary to Gray code converter:-

BINARY				GRAY			
B3	**B2**	**B1**	**B0**	**G3**	**G2**	**G1**	**G0**
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0				
1	1	0	1				
1	1	1	0				
1	1	1	1				

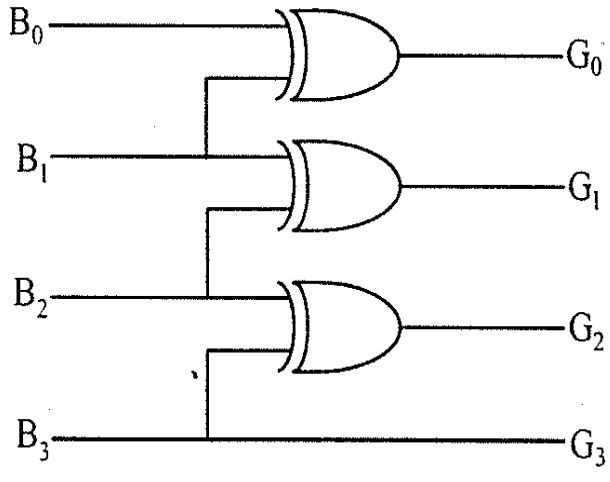
K-Map for G_3:

K-Map for G_2:

K-Map for G_1:

K-Map for G_0:

Logic diagram



4-bit gray to binary code converter:-

| **Gray Code** | **Binary Code** |

G3	**G2**	**G1**	**G0**	**B3**	**B2**	**B1**	**B0**
0	**0**	**0**	**0**				
0	**0**	**0**	**1**				
0	**0**	**1**	**1**				
0	**0**	**1**	**0**				
0	**1**	**1**	**0**				
0	**1**	**1**	**1**				
0	**1**	**0**	**1**				
0	**1**	**0**	**0**				
1	**1**	**0**	**0**				
1	**1**	**0**	**1**				
1	**1**	**1**	**1**				
1	**1**	**1**	**0**				
1	**0**	**1**	**0**				
1	**0**	**1**	**1**				
1	**0**	**0**	**1**				
1	**0**	**0**	**0**				

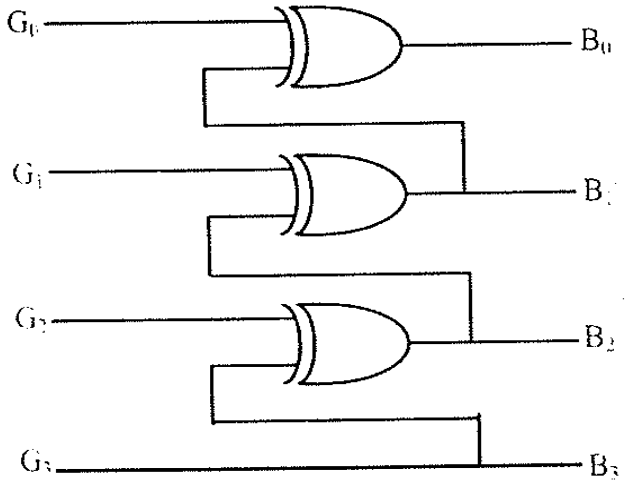
K-Map for B_3:

K-Map for B_2:

K-Map for B_1:

K-Map for B_0:

Logic diagram



PROCEDURE

Test all the components and IC packages using multimeter or digital IC tester.

Set up the regulated circuit of converters.

Verify the truth tables by producing required different input combinations of digits.

RESULT

EXPERIMENT 10

II. BCD TO EXCESS 3 CODE & EXCESS 3 TO BCD CONVERTER

Aim

To study and Verify the BCD to Excess-3 code converter & Excess 3 to BCD converter using logic gates.

Procedure

Place the IC on IC Trainer Kit.

Connect VCC and ground to respective pins of IC Trainer Kit.

Implement the circuit as shown in the circuit diagram.

Connect the inputs to the input switches provided in the IC Trainer Kit.

Connect the outputs to the switches of O/P LEDs

Apply various combinations of inputs according to the truth table and observe the condition of LEDs.

Note down the corresponding output readings for various combinations of inputs.

Power Off Trainer Kit, disconnect all the wire connections and remove IC's from IC-Base.

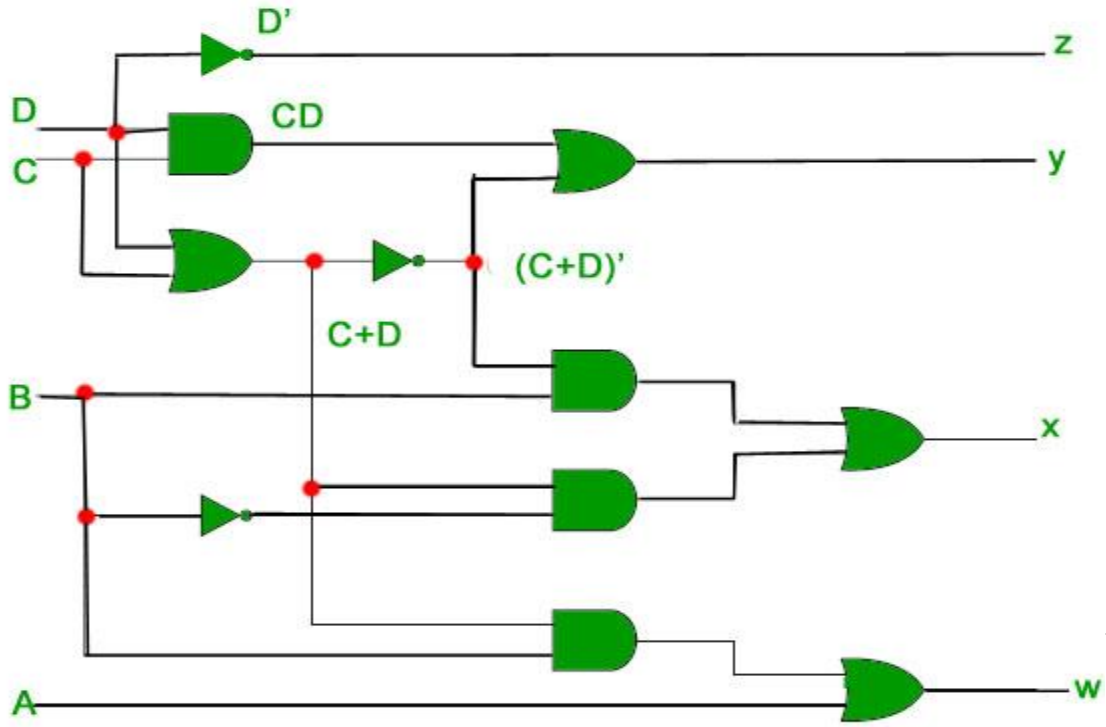
Theory

Binary Coded Decimal (BCD) Code - Digital numbers are represented, stored and transmitted as group of binary bits. This group is also called as binary code decimals. Weighted binary codes are those binary codes which obey the positional weight principle. Each position of the number represents a specific weight. Several systems of the codes are used to express the decimal digits 0 through 9. In these codes each decimal digit is represented by a group of four bits.

In this code each decimal digit is represented by a 4-bit binary number. BCD is a way to express each of the decimal digits with a binary code. In the BCD, with four bits we can represent sixteen numbers (0000 to 1111). But in BCD code only first ten of these are used (0000 to 1001). The remaining six code combinations i.e. 1010 to 1111 are invalid in BCD.

BCD				EXCESS 3			
A	B	C	D	w	x	y	z

Circuit Diagram



Converting Excess 3 to BCD

Excess 3				BCD			
w	x	y	z	A	B	C	D

K-Map for D-

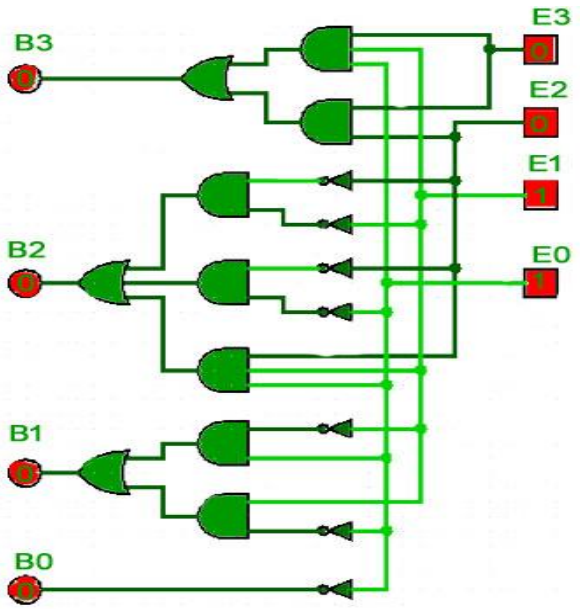
K-Map for C-

K-Map for B-

K-Map for A-

The corresponding digital circuit –

Here $E_3,\ E_2,\ E_1,\ and\ E_0$ correspond to $w,\ x,\ y,\ and\ z$ and $B_3,\ B_2,\ B_1,\ and\ B_0$ correspond to $A,\ B,\ C,\ and\ D$.



RESULT

EXPERIMENT 11

MULTIPLEXER AND DEMULTIPLEXER

AIM:

To design and set up the following circuit

1) To design and set up a 4:1 Multiplexer (MUX) using only NAND gates.

2) To design and set up a 1:4 Demultiplexer(DE-MUX) using only NAND gates.

THEORY

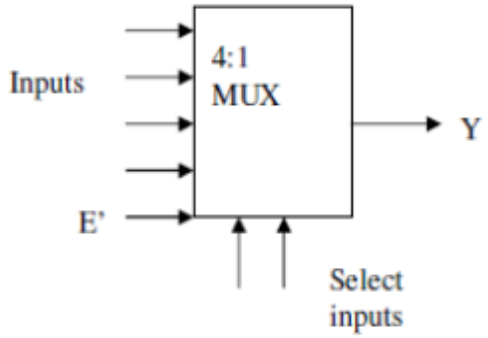
Multiplexers are very useful components in digital systems. They transfer a large number of information units over a smaller number of channels, (usually one channel) under the control of selection signals. Multiplexer means many to one. A multiplexer is a circuit with many inputs but only one output. By using control signals (select lines) we can select any input to the output. Multiplexer is also called as data selector because the output bit depends on the input data bit that is selected. The general multiplexer circuit has 2^n input signals, n control/select signals and 1 output signal.

De-multiplexers perform the opposite function of multiplexers. They transfer a small number of information units (usually one unit) over a larger number of channels under the control of selection signals. The general de-multiplexer circuit has 1 input signal, n control/select signals and 2^n output signals. De-multiplexer circuit can also be realized using a decoder circuit with enable.

COMPONENTS REQUIRED:

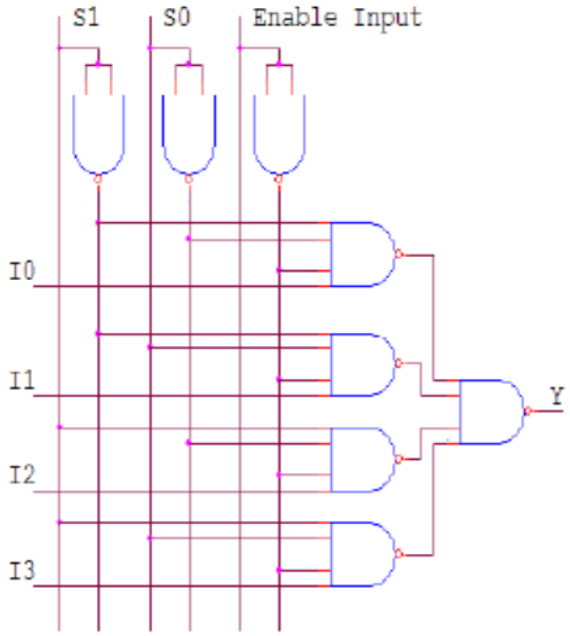
IC 7400, IC 7410, IC 7420, IC 7404, IC 74153, IC 74139, Patch Cords & IC Trainer Kit.

i) 4:1 MULTIPLEXER



Output Y= E'S1'S0'I0 + E'S1'S0I1 + E'S1S0'I2 + E'S1S0I3

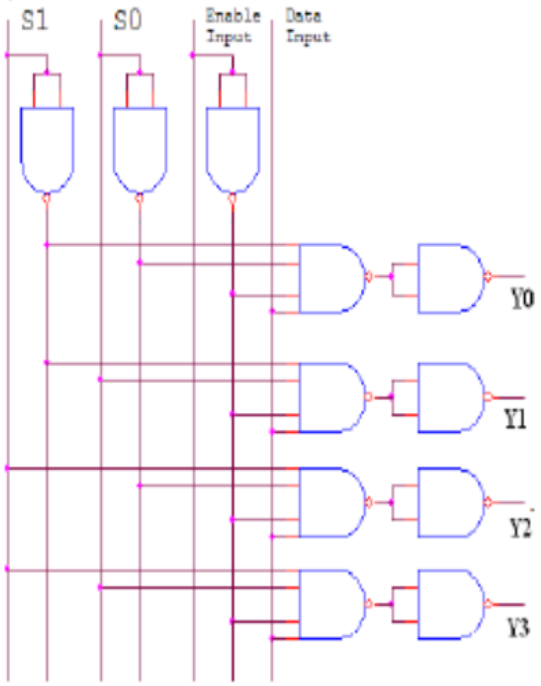
REALIZATION USING NAND GATES



TRUTH TABLE

Select Inputs		Enable Input	Inputs				Out puts
S_1	S_0	E	I_0	I_1	I_2	I_3	Y
X	X	1	X	X	X	X	0
0	0	0	0	X	X	X	0
0	0	0	1	X	X	X	1
0	1	0	X	0	X	X	0
0	1	0	X	1	X	X	1
1	0	0	X	X	0	X	0
1	0	0	X	X	1	X	1
1	1	0	X	X	X	0	0
1	1	0	X	X	X	1	1

ii) DE-MUX USING NAND GATES



Enable Inputs	Data Input	Select Inputs		Outputs			
E	D	S_1	S_0	Y_3	Y_2	Y_1	Y_0
1	0	X	X	X	X	X	X
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	1	0	0
0	1	1	1	1	0	0	0

PROCEDURE:

• Check all the components for their working.

• Insert the appropriate IC into the IC base.

• Make connections as shown in the circuit diagram.

• Verify the Truth Table and observe the outputs.

RESULT

EXPERIMENT 12

DECODERS AND ENCODERS

Aim

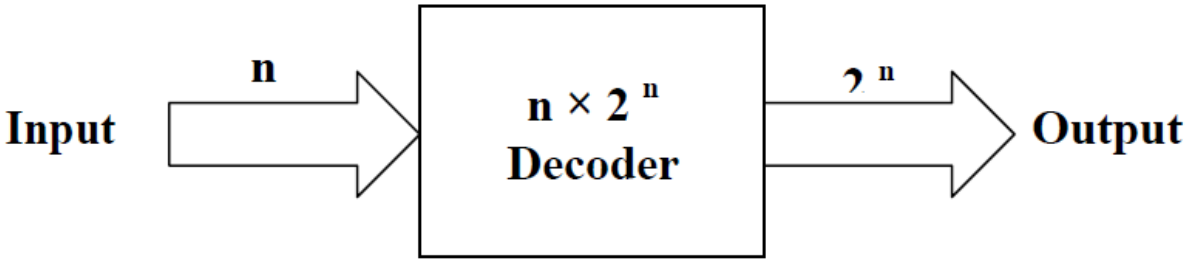
To be familiar with basics of conversion from binary to decimal by using decoder networks.

Theory

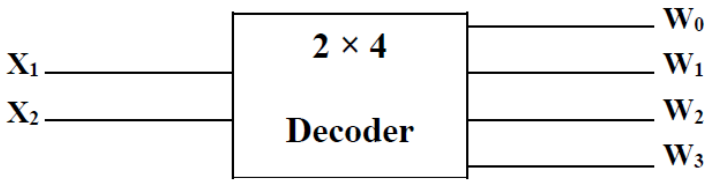
1. Decoder

The process of taking some type of code and determining what it represents in terms of a recognizable number or character is called decoding. A decoder is a combinational logic circuit that performs the decoding function, and produce an output that indicates the (meaning) of the input code.

The decoder is an important part of the system which selects the cells to be read from and write into. This particular circuit is called a decoder matrix, or simply a decoder, and has a characteristic that for each of the possible 2n binary input number which can be taken by the n input cells, the matrix will have a unique one of its 2n output lines selected.



The decoder is called n to m where m < 2n for example two to four line decoder, Fig. shows a two to four line decoder and its truth table



INPUTS		OUTPUTS			
X_2	X_1	W_0	W_1	W_2	W_3
0	0				
0	1				
1	0				
1	1				

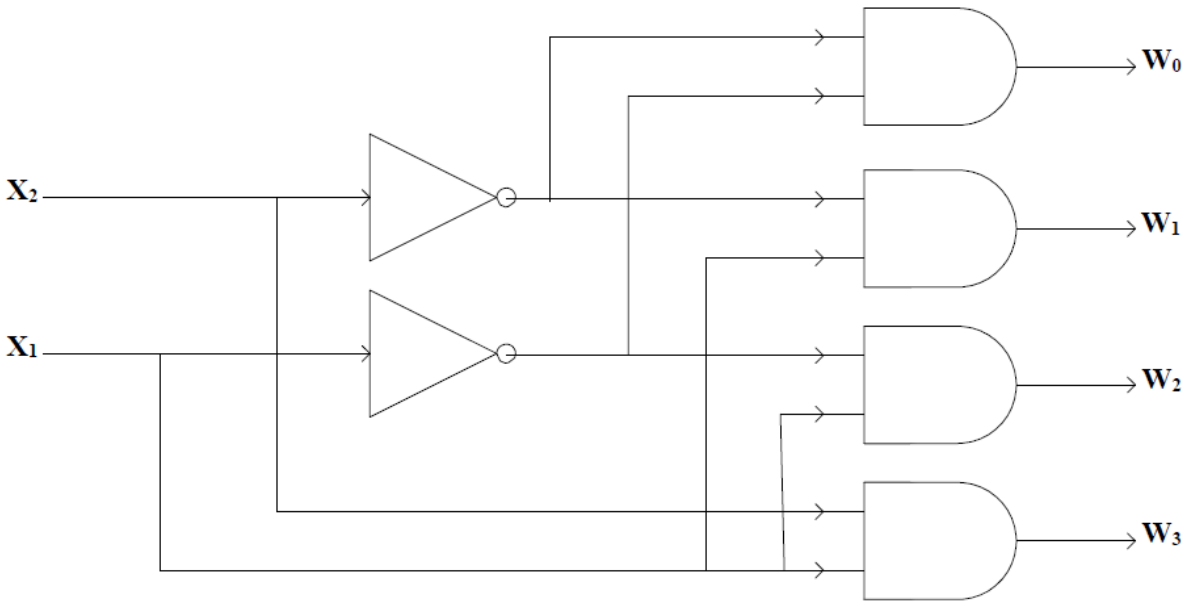
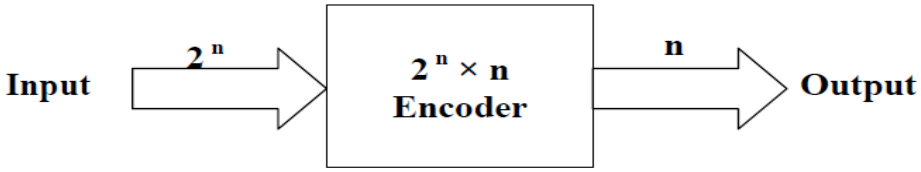


Fig. (1)
Two to Four Line Decoder

2. Encoder

An encoder is a combinational logic circuit that generate n output lines from 2n (or less) inputs. It has the reverse function of the decoder.



An encoder accepts digit on its inputs, such as a decimal or octal digit, and converts it to a coded output, such as a binary or BCD. Encoder can also be devised to encode various symbol and alphabetic characters. This process of converting from familiar symbols or numbers to a coded format is called encoding.

Figure shown a four to two line encoder and its truth table.

INPUTS				OUTPUTS	
W_3	W_2	W_1	W_0	X_2	X_1
0	0	0	1		
0	0	1	0		
0	1	0	0		
1	0	0	0		

Table (3)
Truth Table of Four to Two Line Encoder.

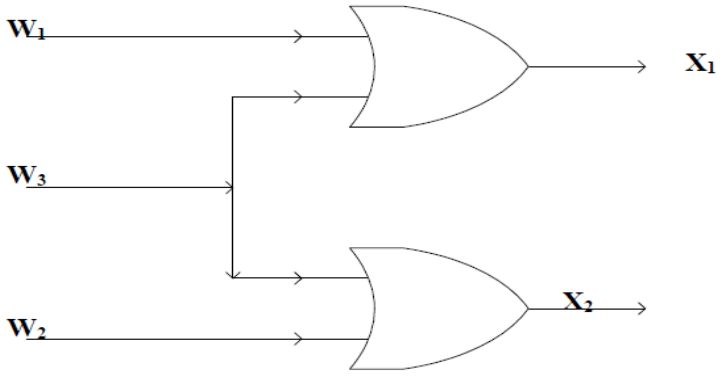


Fig. (3)
Four to Two line Encoder

PROCEDURE:

• Check all the components for their working.

• Insert the appropriate IC into the IC base.

• Make connections as shown in the circuit diagram.

• Verify the Truth Table and observe the outputs.

RESULT

EXPERIMENT 13

DESIGN AND IMPLEMENTATION OF SHIFT REGISTER USING FLIP FLOPS

AIM:

To design and implement the following shift register

(i) Serial in serial out
(ii) Serial in parallel out
(iii) Parallel in serial out
(iv) Parallel in parallel out

COMPONENTS AND EQUIPMENT REQUIRED

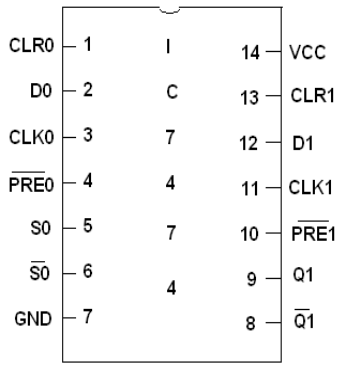
IC 7474, IC 7432 & IC TRAINER KIT

THEORY:

A register is capable of shifting its binary information in one or both directions is known as shift register. The logical configuration of shift register consist of a D-Flip flop cascaded with output of one flip flop connected to input of next flip flop. All flip flops receive common clock pulses which causes the shift in the output of the flip flop.

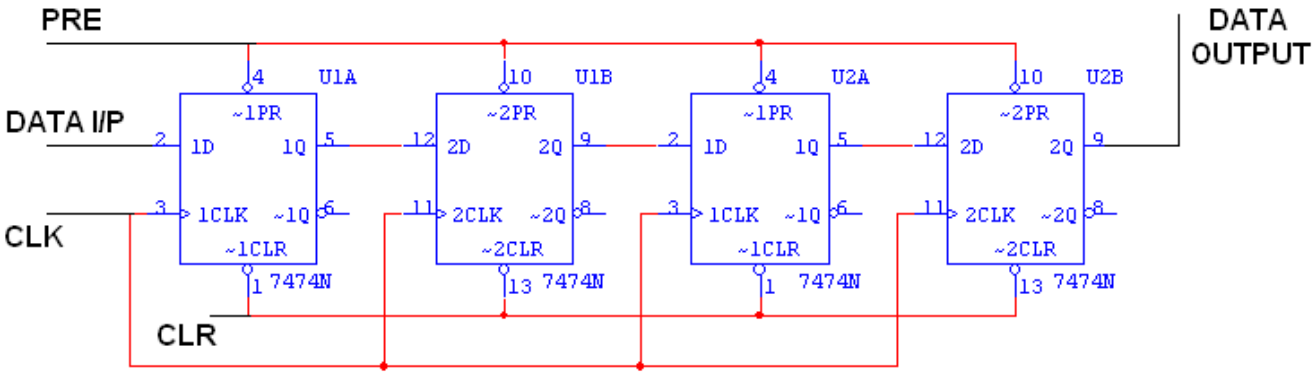
The simplest possible shift register is one that uses only flip flop. The output of a given flip flop is connected to the input of next flip flop of the register. Each clock pulse shifts the content of register one bit position to right.

PIN DIAGRAM:



LOGIC DIAGRAM:

SERIAL IN SERIAL OUT:



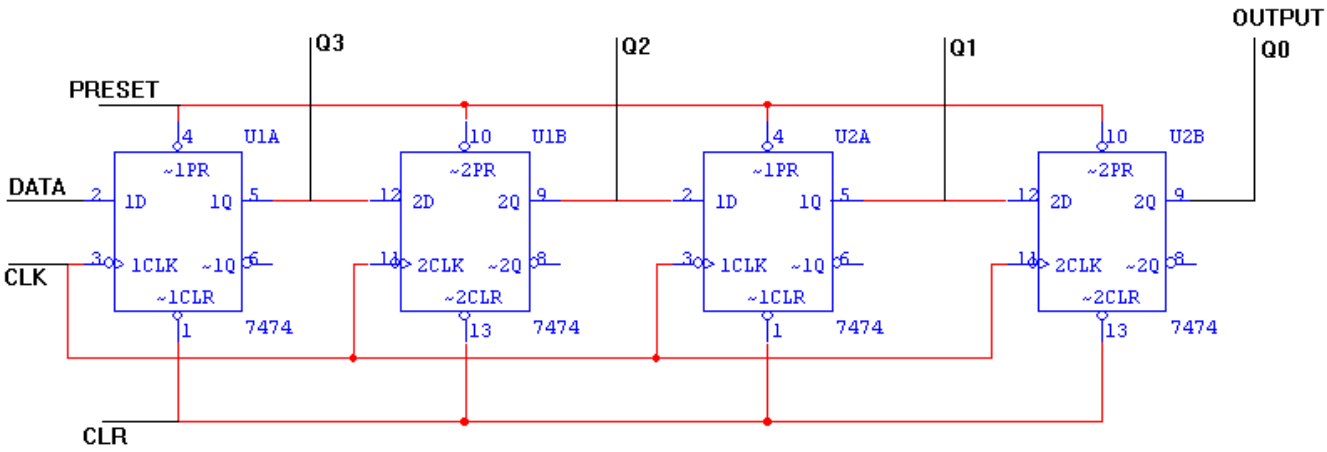
TRUTH TABLE:

CLK	Serial in	Serial out
1	**1**	**0**
2	**0**	**0**
3	**0**	**0**
4	**1**	**1**

5	X	0
6	X	0
7	X	1

LOGIC DIAGRAM:

SERIAL IN PARALLEL OUT:



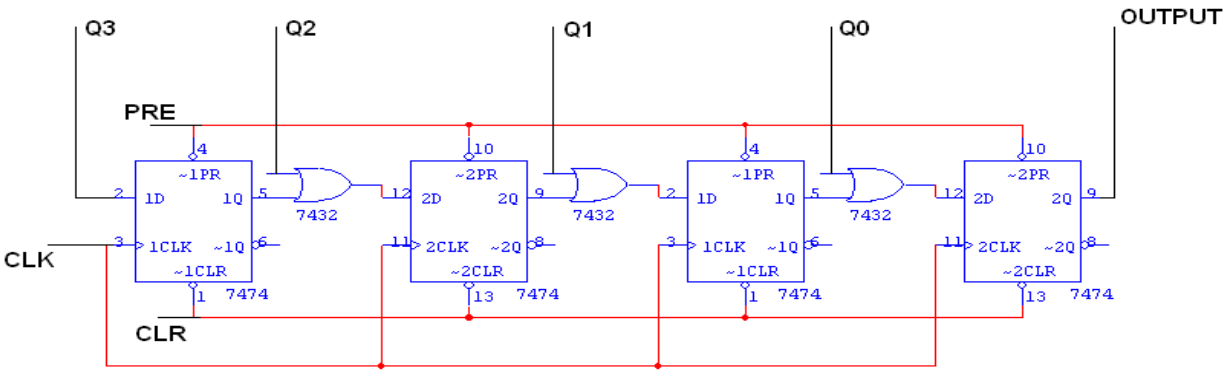
TRUTH TABLE:

CLK	DATA	OUTPUT			
		Q_A	Q_B	Q_C	Q_D
1	1				
2	0				

3	0				
4	1				

LOGIC DIAGRAM:

PARALLEL IN SERIAL OUT:

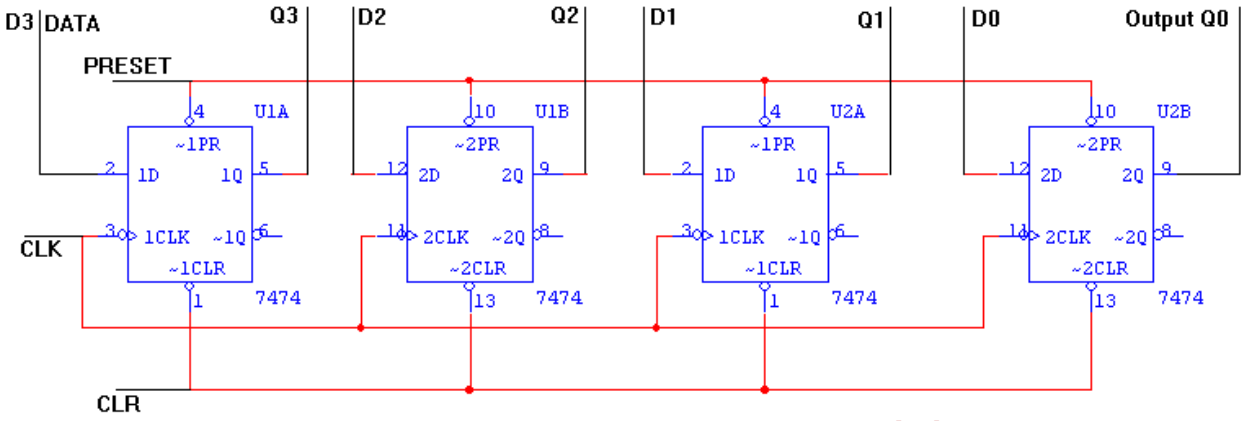


TRUTH TABLE:

CLK	Q3	Q2	Q1	Q0	O/P
0	1	0	0	1	
1	0	0	0	0	
2	0	0	0	0	
3	0	0	0	0	

LOGIC DIAGRAM:

PARALLEL IN PARALLEL OUT:



TRUTH TABLE:

CLK	DATA INPUT				OUTPUT			
	D_A	D_B	D_C	D_D	Q_A	Q_B	Q_C	Q_D
1	1	0	0	1				
2	1	0	1	0				

PROCEDURE:

1. Connections are given as per circuit diagram.
2. Logical inputs are given as per circuit diagram.
3. Observe the output and verify the truth table.

RESULT:

EXPERIMENT 14

3 BIT SYNCHRONOUS & ASYNCHRONOUS COUNTERS

AIM:

To design and implement Asynchronous and synchronous counters

COMPONENTS AND EQUIPMENTS REQUIRED

IC-7476 & IC Trainer Kit

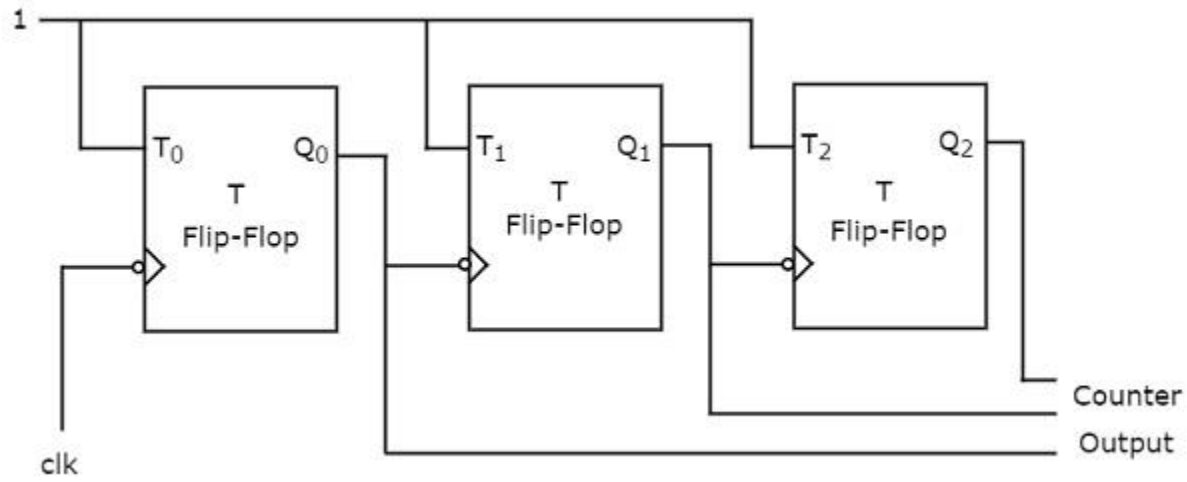
THEORY

Asynchronous Counters

If the flip-flops do not receive the same clock signal, then that counter is called as **Asynchronous counter**. The output of system clock is applied as clock signal only to first flip-flop. The remaining flip-flops receive the clock signal from output of its previous stage flip-flop. Hence, the outputs of all flip-flops do not change affect at the same time.

Asynchronous Binary Up Counter

An 'N' bit Asynchronous binary up counter consists of 'N' T flip-flops. It counts from 0 to $2^N - 1$. The **block diagram** of 3-bit Asynchronous binary up counter is shown in the following figure.



The 3-bit Asynchronous binary up counter contains three T flip-flops and the T-input of all the flip-flops are connected to '1'. All these flip-flops are negative edge triggered but the outputs change asynchronously. The clock signal is directly applied to the first T flip-flop. So, the output of first T flip-flop **toggles** for every negative edge of clock signal.

The output of first T flip-flop is applied as clock signal for second T flip-flop. So, the output of second T flip-flop toggles for every negative edge of output of first T flip-flop. Similarly, the output of third T flip-flop toggles for every negative edge of output of second T flip-flop, since the output of second T flip-flop acts as the clock signal for third T flip-flop.

Assume the initial status of T flip-flops from rightmost to leftmost is Q2Q1Q0=000. Here, Q2 & Q0 are MSB & LSB respectively. We can understand the **working** of 3-bit asynchronous binary counter from the following table.

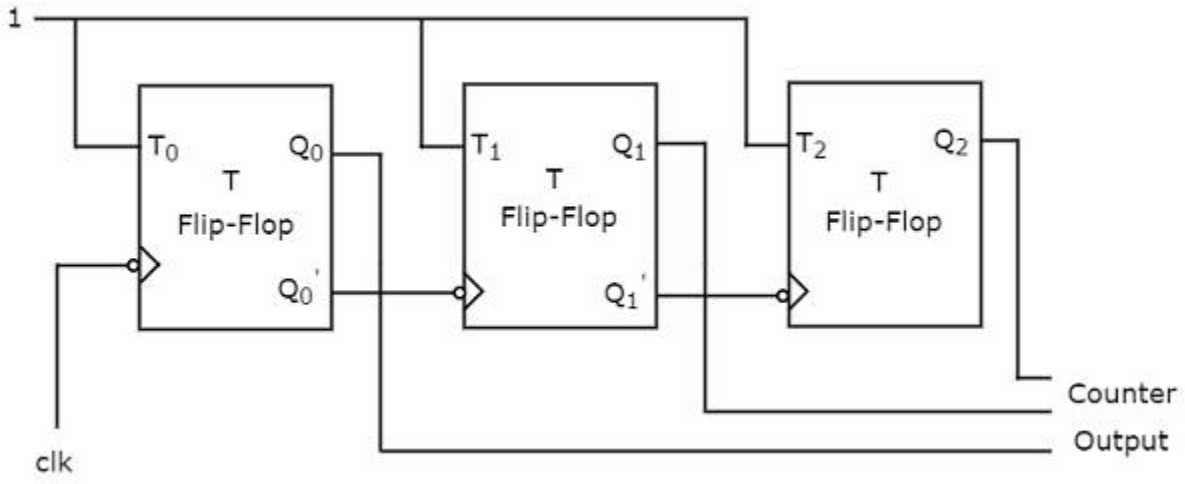
No of negative edge of Clock	**Q_0** -LSB	**Q_1**	**Q_2** - MSB
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1

Here Q0 toggled for every negative edge of clock signal. Q1 toggled for every Q0 that goes from 1 to 0, otherwise remained in the previous state. Similarly, Q2 toggled for every Q1 that goes from 1 to 0, otherwise remained in the previous state.

The initial status of the T flip-flops in the absence of clock signal is Q2Q1Q0=000. This is incremented by one for every negative edge of clock signal and reached to maximum value at 7th negative edge of clock signal. This pattern repeats when further negative edges of clock signal are applied.

Asynchronous Binary Down Counter

An 'N' bit Asynchronous binary down counter consists of 'N' T flip-flops. It counts from $2^N - 1$ to 0. The **block diagram** of 3-bit Asynchronous binary down counter is shown in the following figure.



The block diagram of 3-bit Asynchronous binary down counter is similar to the block diagram of 3-bit Asynchronous binary up counter. But, the only difference is that instead of connecting the normal outputs of one stage flip-flop as clock signal for next stage flip-flop, connect the **complemented outputs** of one stage flip-flop as clock signal for next stage flip-flop. Complemented output goes from 1 to 0 is same as the normal output goes from 0 to 1.

Assume the initial status of T flip-flops from rightmost to leftmost is Q2Q1Q0=000. Here, Q2 & Q0 are MSB & LSB respectively. We can understand the **working** of 3-bit asynchronous binary down counter from the following table.

No of negative edge of Clock	**Q_0 - LSB**	**Q_1**	**Q_2 - MSB**
0	0	0	0
1	1	1	1
2	0	1	1
3	1	0	1
4	0	0	1

5	1	1	0
6	0	1	0
7	1	0	0

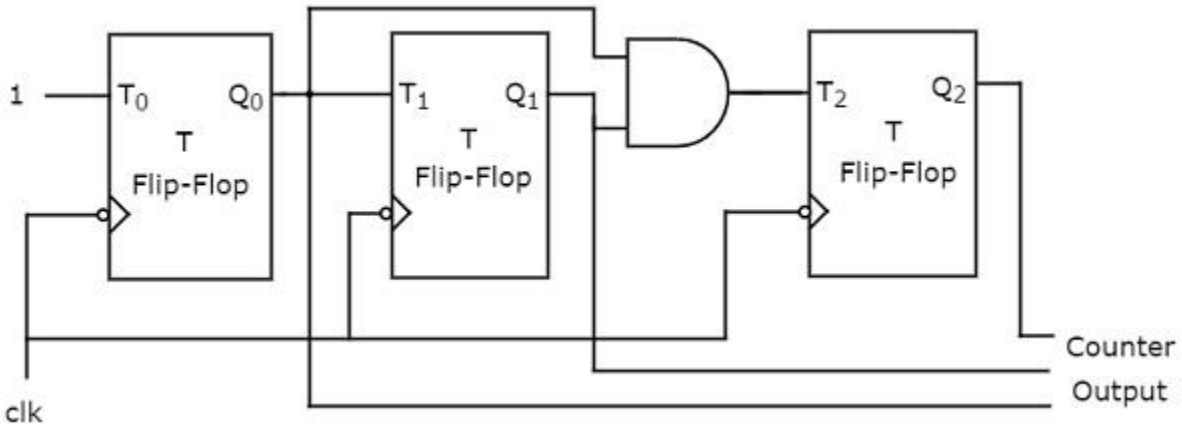
Here Q0 toggled for every negative edge of clock signal. Q1 toggled for every Q0 that goes from 0 to 1, otherwise remained in the previous state. Similarly, Q2 toggled for every Q1 that goes from 0 to 1, otherwise remained in the previous state.
The initial status of the T flip-flops in the absence of clock signal is Q2Q1Q0=000. This is decremented by one for every negative edge of clock signal and reaches to the same value at 8^{th} negative edge of clock signal. This pattern repeats when further negative edges of clock signal are applied.

Synchronous Counters

If all the flip-flops receive the same clock signal, then that counter is called as **Synchronous counter**. Hence, the outputs of all flip-flops change affectaffect at the same time.

Synchronous Binary Up Counter

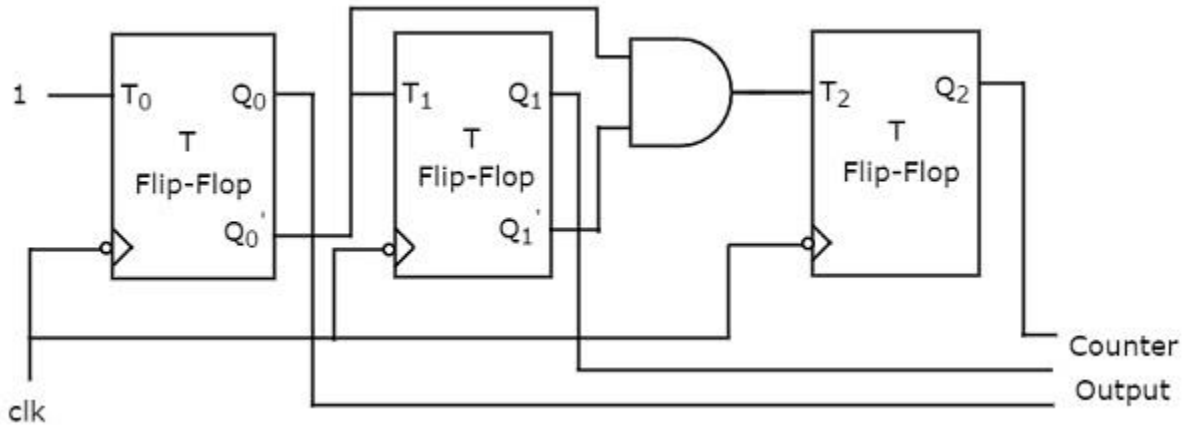
An 'N' bit Synchronous binary up counter consists of 'N' T flip-flops. It counts from 0 to $2^N - 1$. The **block diagram** of 3-bit Synchronous binary up counter is shown in the following figure.



The 3-bit Synchronous binary up counter contains three T flip-flops & one 2-input AND gate. All these flip-flops are negative edge triggered and the outputs of flip-flops change affect synchronously. The T inputs of first, second and third flip-flops are 1, Q0 & Q1Q0 respectively.
The output of first T flip-flop **toggles** for every negative edge of clock signal. The output of second T flip-flop toggles for every negative edge of clock signal if Q0 is 1. The output of third T flip-flop toggles for every negative edge of clock signal if both Q0 & Q1 are 1.

Synchronous Binary Down Counter

An 'N' bit Synchronous binary down counter consists of 'N' T flip-flops. It counts from $2^N - 1$ to 0. The **block diagram** of 3-bit Synchronous binary down counter is shown in the following figure.



The 3-bit Synchronous binary down counter contains three T flip-flops & one 2-input AND gate. All these flip-flops are negative edge triggered and the outputs of flip-flops change affect synchronously. The T inputs of first, second and third flip-flops are 1, Q0′ & Q1′Q0′ respectively.

The output of first T flip-flop **toggles** for every negative edge of clock signal. The output of second T flip-flop toggles for every negative edge of clock signal if Q0′ is 1. The output of third T flip-flop toggles for every negative edge of clock signal if both Q1′ & Q0′ are 1.

PROCEDURE

1. Test all IC's using a digital IC tester. Also test all wires for continuity using a multi meter or IC trainer
2. Setup the circuit for 3 bit Asynchronous and synchronous counter. connect all the preset pins to+5 V to disable it
3. Clear the entire flip flop outputs initially connecting common clear terminal to logic0'. After the usage of clear pins, connect them to logic '1'. Apply mono pulses. Counter starts counting.
4. Set up other counters in similar way and observe.

RESULT

ADDITIONAL/ADVANCED EXPERIMENTS

EXPERIMENT 1

HALF ADDER

AIM

To design and setup half adder using

i) XOR and NAND Gates
ii) NAND Gates only

PRINCIPLE:

A combinational circuit that performs the addition of two bits is called a half adder. One that performs the addition of three bits (two bits and a previous carry) is a full adder.

HALF ADDER: $s = x'y + xy' = x \oplus y$

$c = xy$

MATERIALS REQUIRED

Trainer kit, IC 7400, 7486.

The experimental procedure adopted is given below

1. Verify whether all the components are in good condition.
2. Setup the half added circuit and feed the output bit combination.
3. Observe the output corresponding to input combination and enter it in the truth table.
4. Repeat the above step for full added circuit.

HALF ADDER

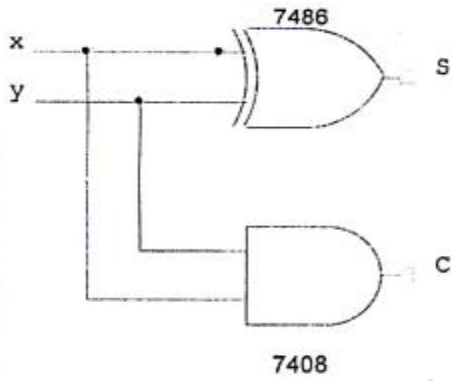
DESIGN

TRUTH TABLE

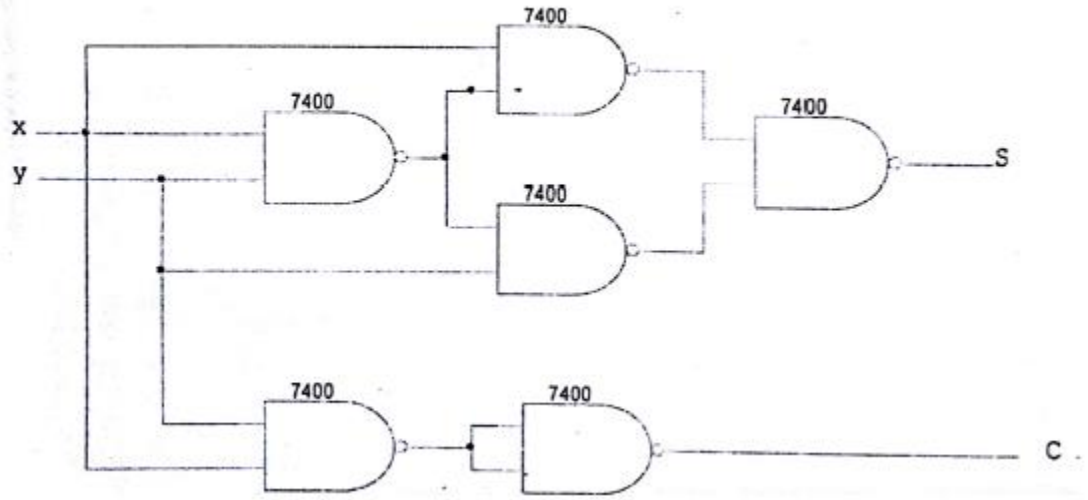
Input		Output	
x	y	s	c
0	0		
0	1		
1	0		
1	1		

$s = x'y + xy' = x \oplus y$ = x Ex Or y

HALF ADDER USING XOR & AND GATES



HALF ADDER USING NAND GATES ONLY



RESULT

INFERENCE

EXPERIMENT 2

HALF SUBTRACTOR

AIM

To design and setup half subtractor using

i) XOR and NAND Gates
ii) NAND Gates only

APPARATUS REQUIRED:

1. IC 7408, 7486 , 7432 , 7404
2. IC Trainer Kit

PRINCIPLE:

A combinational circuit that performs the subtraction of two bits is called a half subtractor. One that performs the subtraction of three bits (two bits and a borrow) is a full subtractor.

MATERIALS REQUIRED

The following components and equpiments are used for half subtractor.

Trainer kit, IC 7400,7486.IC

The experimental procedure adopted is given below

1. Verify whether all the components are in good condition.
2. Setup the half subtracted circuit and feed the input bit combination.
3. Observe the output corresponding to input combination and enter it in the truth table.
4. Repeat the above step for full subtractor circuit.

PROCEDURE:

1. Test all the components and IC trainer packages using a digital IC tester.
2. Assure whether all the connection wires are in good condition by testing for the continuity using multimeter or a trainer kit. Continuity of wires can be tested using trainer kit by shorting a 5v supply in trainer kit to an LED. If wires are in good condition LED will Glow.
3. Verify the dual in line pin out of the IC before feeding the input.
4. Connect the circuit as given in the circuit diagram.
5. Verify the truth table of the circuit.

DESIGN

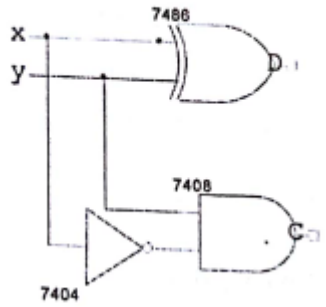
Truth Table

Input		Output	
x	y	s	c
0	0		
0	1		
1	0		
1	1		

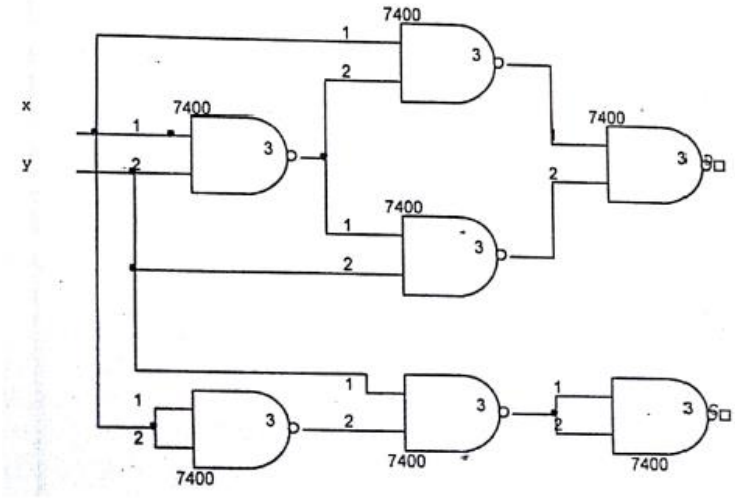
$D = x'y + xy' = x \ominus y$

$c = x'y$

Half Subtractor using XOR and basic gates



Half Subtractor using NAND gates only



RESULT

INFERENCE